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Shim et al.

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(54) **CONTROL METHOD OF NONVOLATILE MEMORY DEVICE**

(71) Applicants: **Sunil Shim**, Seoul (KR); **Jin-Man Han**, Seongnam-si (KR); **Sang-Wan Nam**, Hwaseong-si (KR); **Won-Taeck Jung**, Hwaseong-si (KR)

(72) Inventors: **Sunil Shim**, Seoul (KR); **Jin-Man Han**, Seongnam-si (KR); **Sang-Wan Nam**, Hwaseong-si (KR); **Won-Taeck Jung**, Hwaseong-si (KR)

(73) Assignee: **Samsung Electronics Co., Ltd.**, Gyeonggi-do (KR)

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(52) **U.S. Cl.**
CPC ***G11C 16/3418*** (2013.01); ***G11C 16/10*** (2013.01); ***G11C 16/14*** (2013.01);

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(58) **Field of Classification Search**
CPC G11C 16/10; G11C 16/14; G11C 16/16; G11C 16/349; G11C 16/3418; G11C 16/0483; H01L 27/11578; H01L 27/11582; H01L 29/7926
USPC 365/185.11, 185.17, 185.25
See application file for complete search history.

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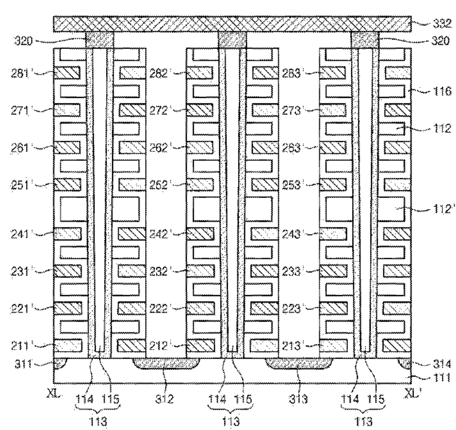
Primary Examiner — Tan T. Nguyen
(74) *Attorney, Agent, or Firm* — Harness, Dickey & Pierce, P.L.C.

(57) **ABSTRACT**

According to example embodiments, a control method of a nonvolatile memory device, which includes a plurality of memory blocks on a substrate, each memory block including a plurality of sub blocks stacked in a direction perpendicular to the substrate and being configured to be erased independently and each sub block including a plurality of memory cells stacked in the direction perpendicular to the substrate. The control method includes comparing a count value of a first memory block with a reference value, the count value determined according to the number of program, read, or erase operations executed at the first memory block after data is programmed in the first memory block; and if the count value is greater than or equal to the reference value, performing a reprogram operation in which data programmed in first the memory block is read and the read data is programmed in a second memory block.

19 Claims, 73 Drawing Sheets



(51) **Int. Cl.**

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G11C 16/16	(2006.01)
H01L 27/115	(2006.01)
H01L 29/792	(2006.01)
G11C 16/14	(2006.01)

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CPC ***G11C 16/16*** (2013.01); ***G11C 16/349*** (2013.01); ***H01L 27/11578*** (2013.01); ***H01L 27/11582*** (2013.01); ***H01L 29/7926*** (2013.01)

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Mar. 25, 2015 US Office Action issued in related U.S. Appl. No. 14/579,755.

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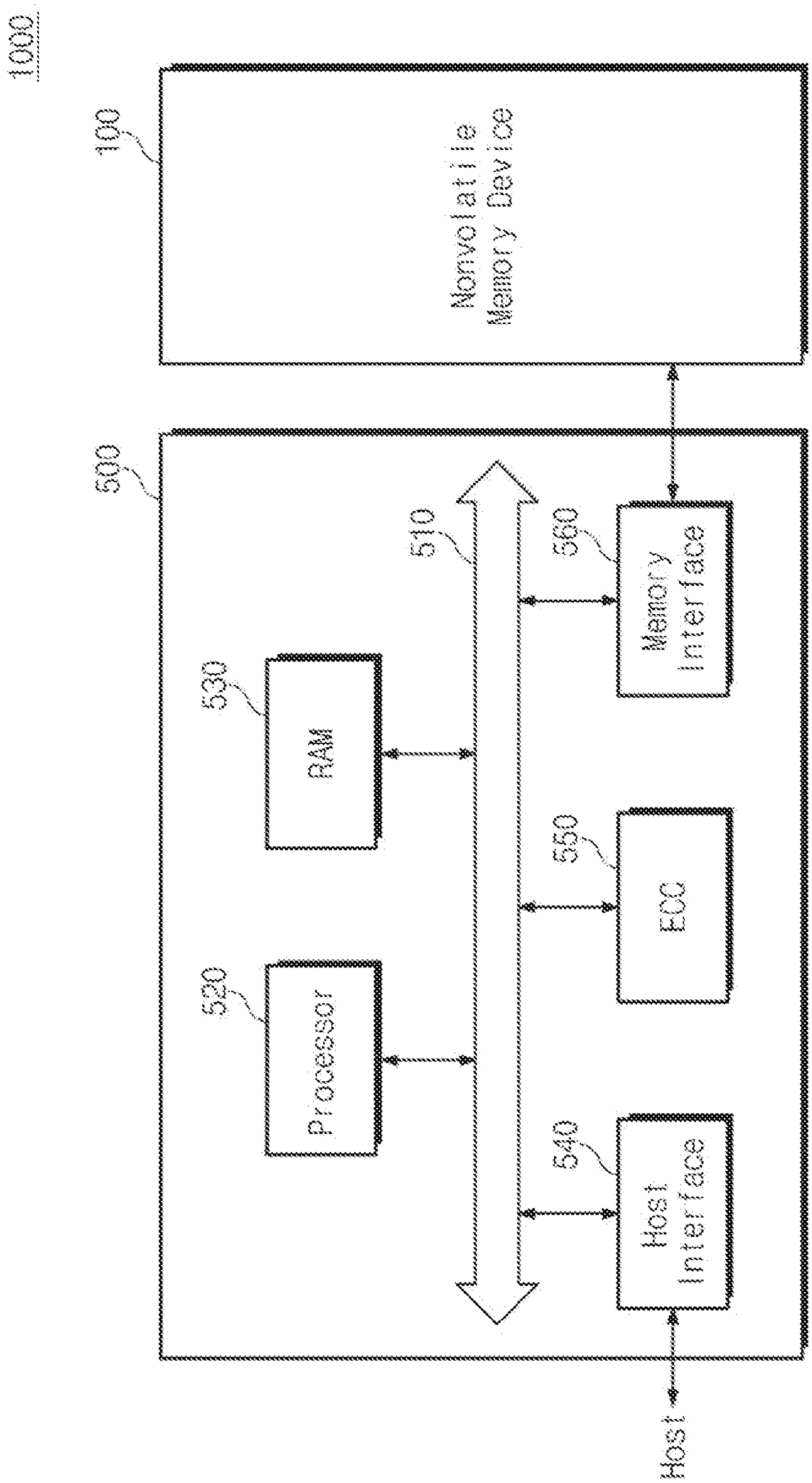
Fig. 1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RAM
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Interface
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ECC
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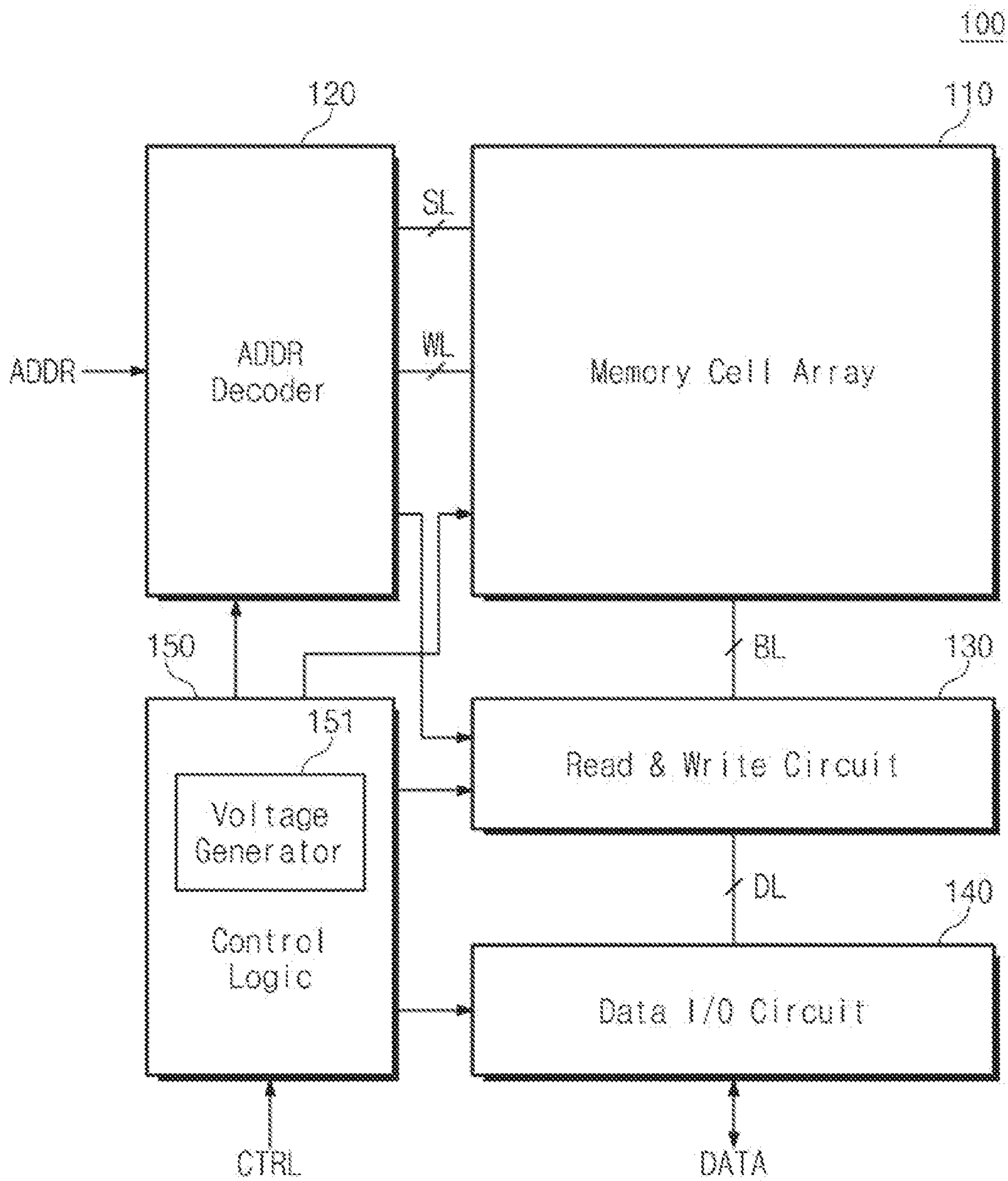
Memory
Interface
Host

Fig. 2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110
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WL
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BL
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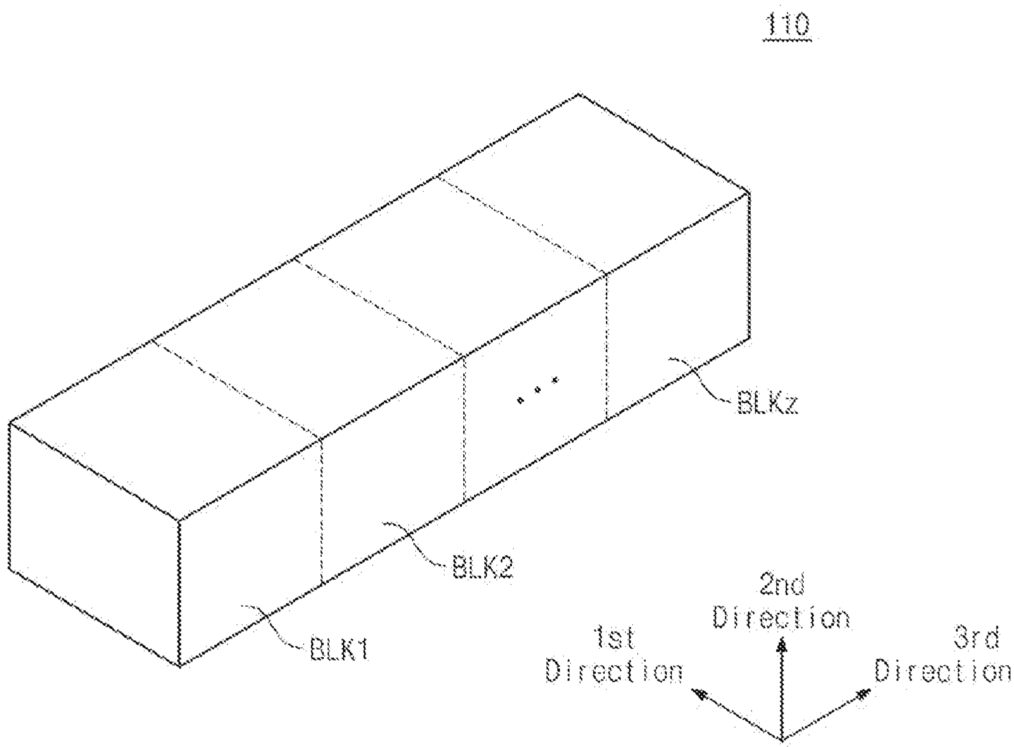
151
Read & Write Circuit
Voltage
Generator
DL
140
Control
Logic
Data I/O Circuit
CTRL
DATA

Fig. 3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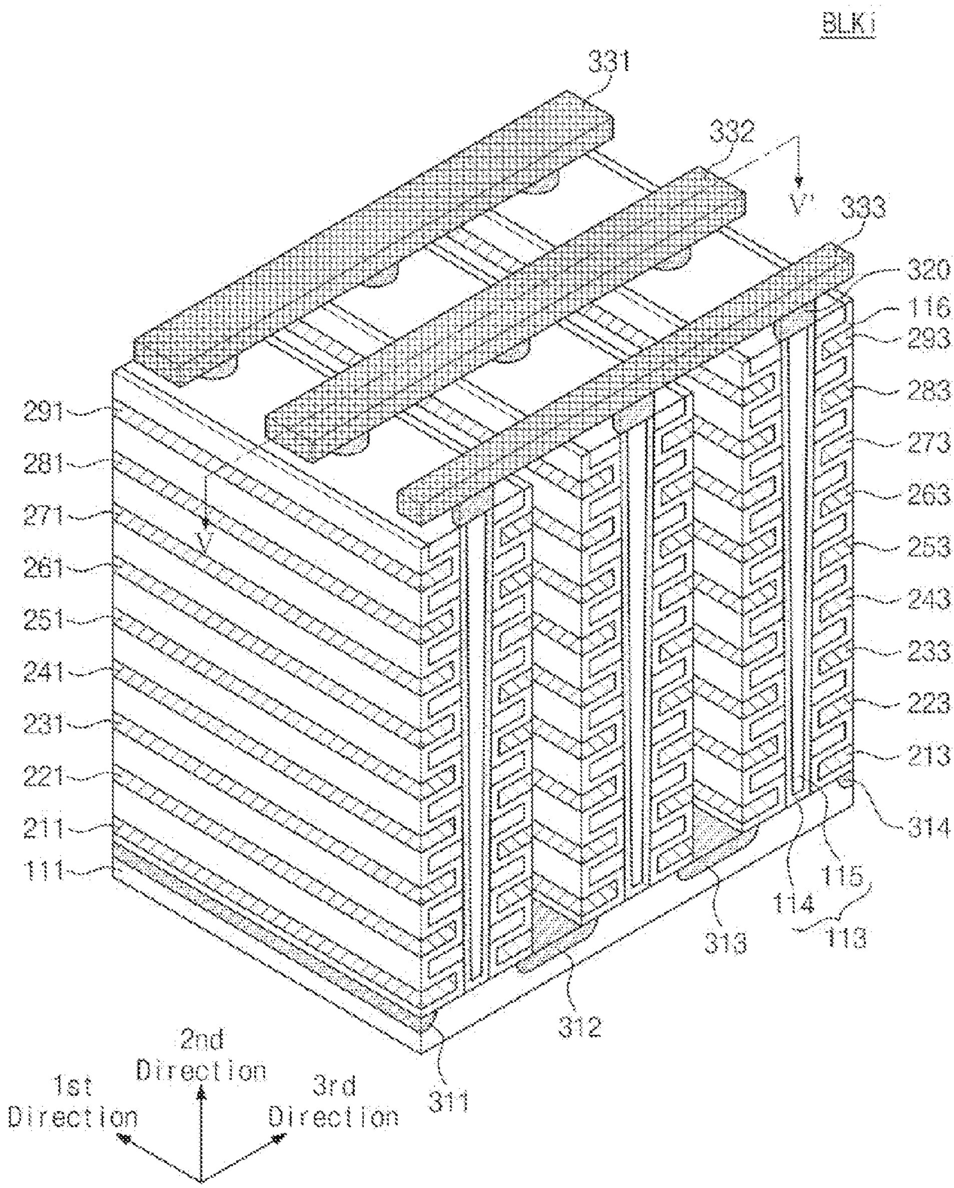
BLK2
BLK1
2nd
Direction
1st
Direction
3rd
Direction

Fig. 4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332
333
V'
V
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271
261
251
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211
111
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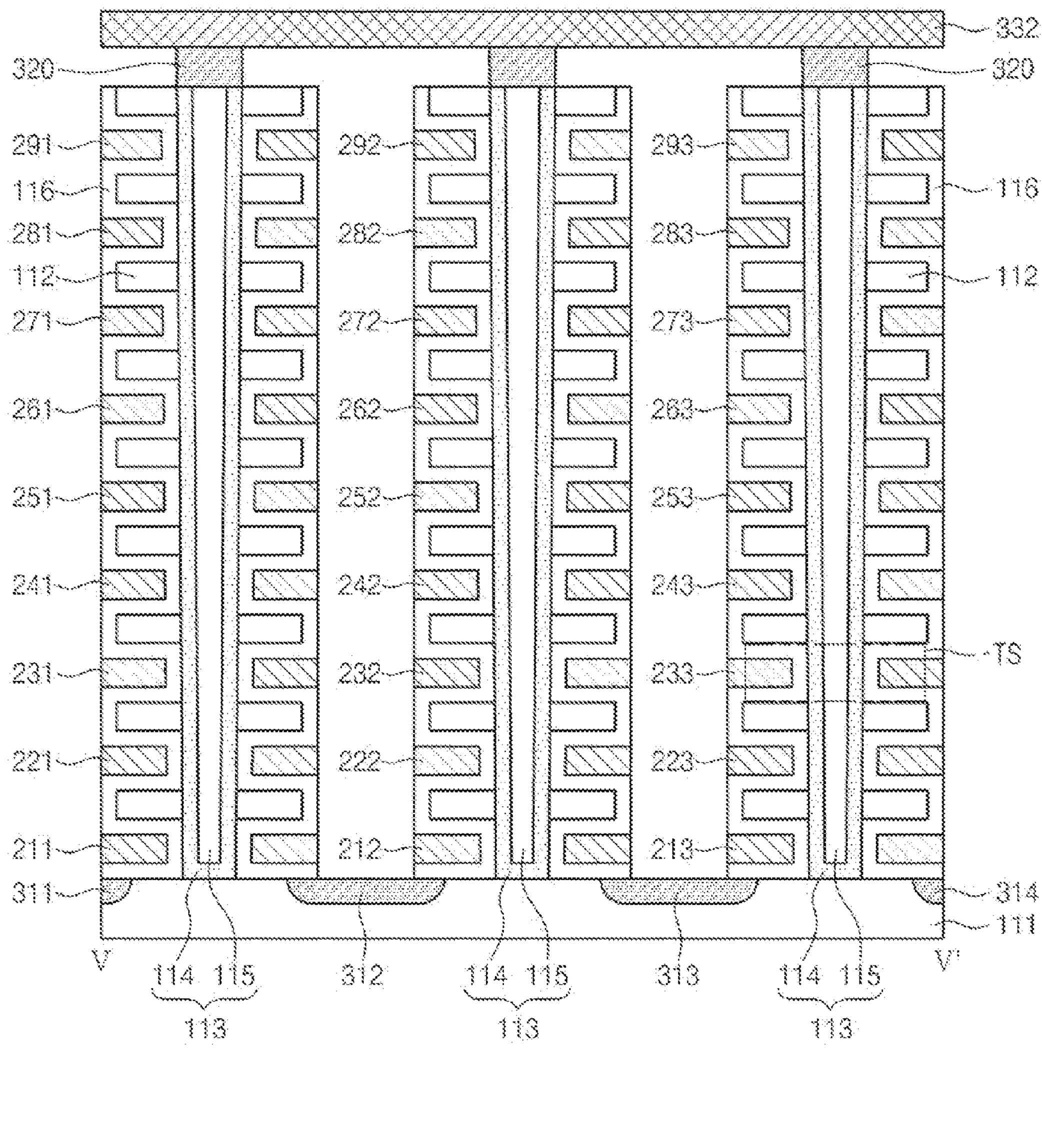
114
113
313
312
311
2nd Direction
1st Direction
3rd Direction

Fig. 5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243
TS
231
232
233
221
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V'
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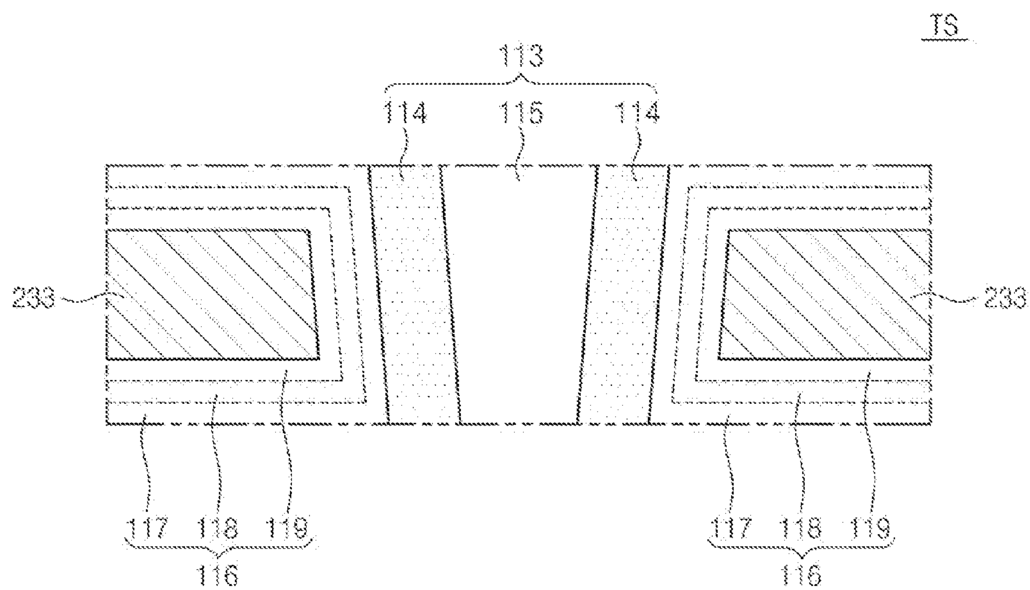
312
114 115
313
114 115
113
113
113

Fig. 6



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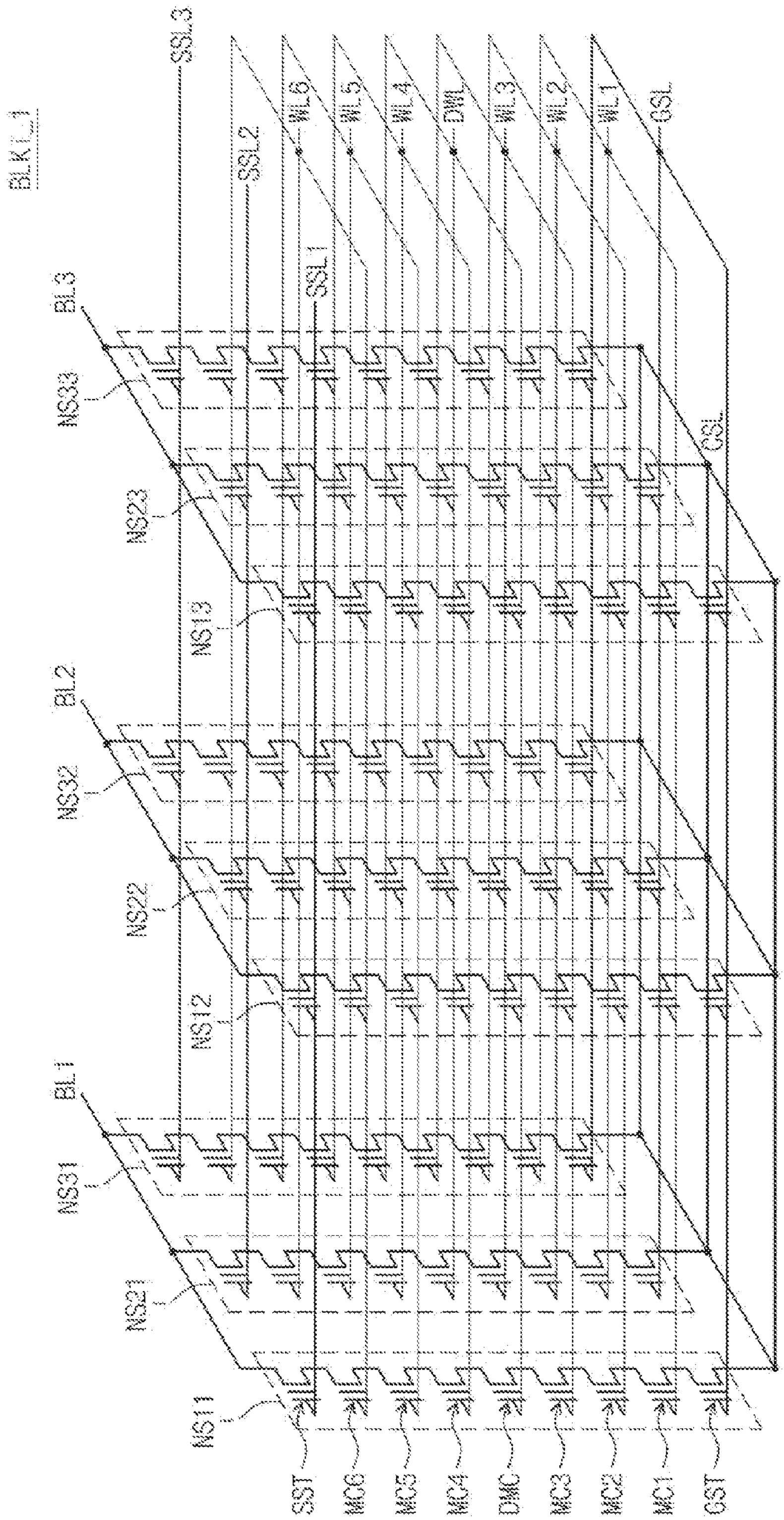
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NS21
NS31
NS12
NS22
NS32
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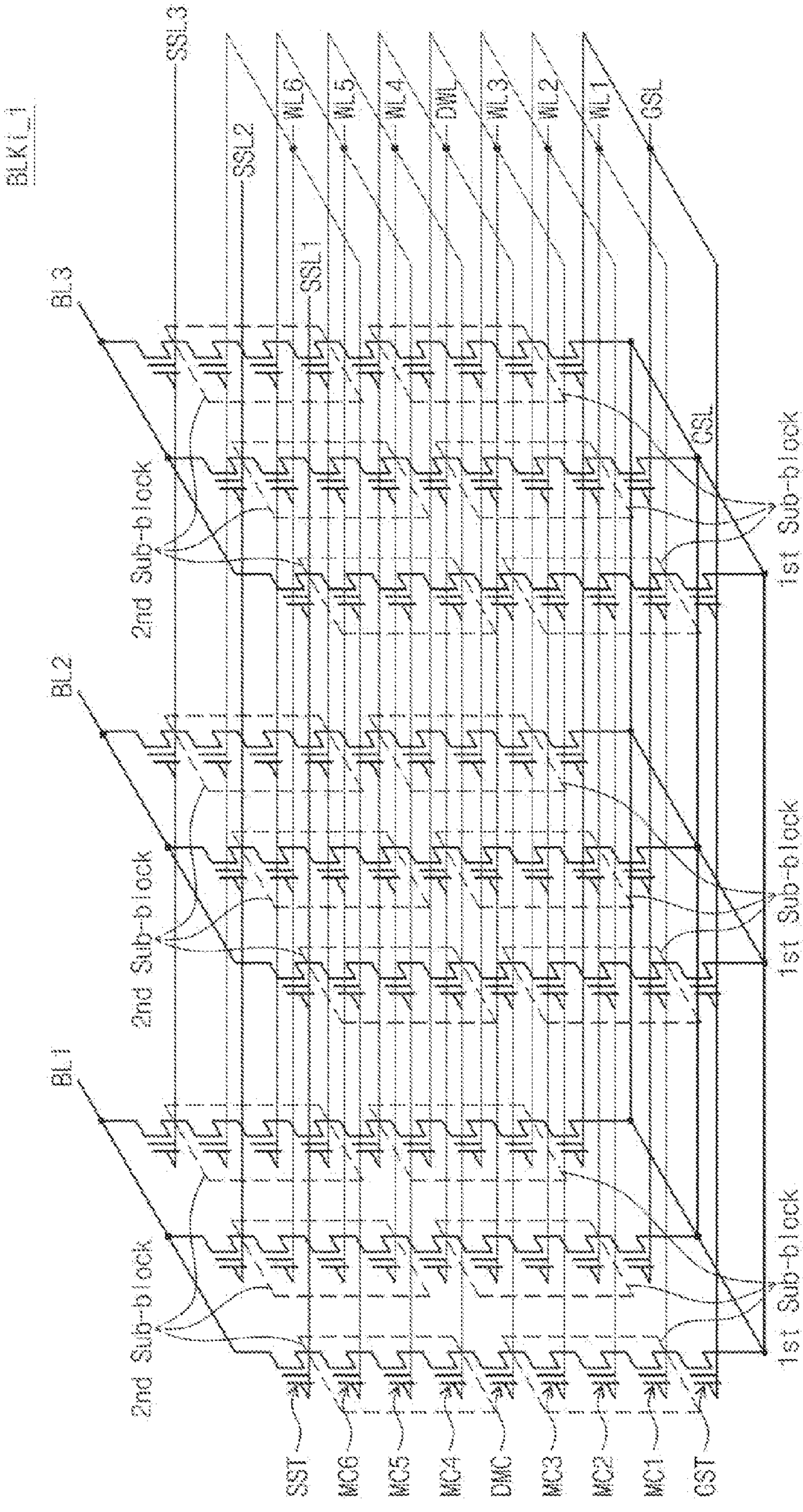
SST
MC6
MC5
MC4
DMC
MC3
MC2
MC1
GST

Fig. 8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WL5
WL4
DWL
WL3
WL2
WL1
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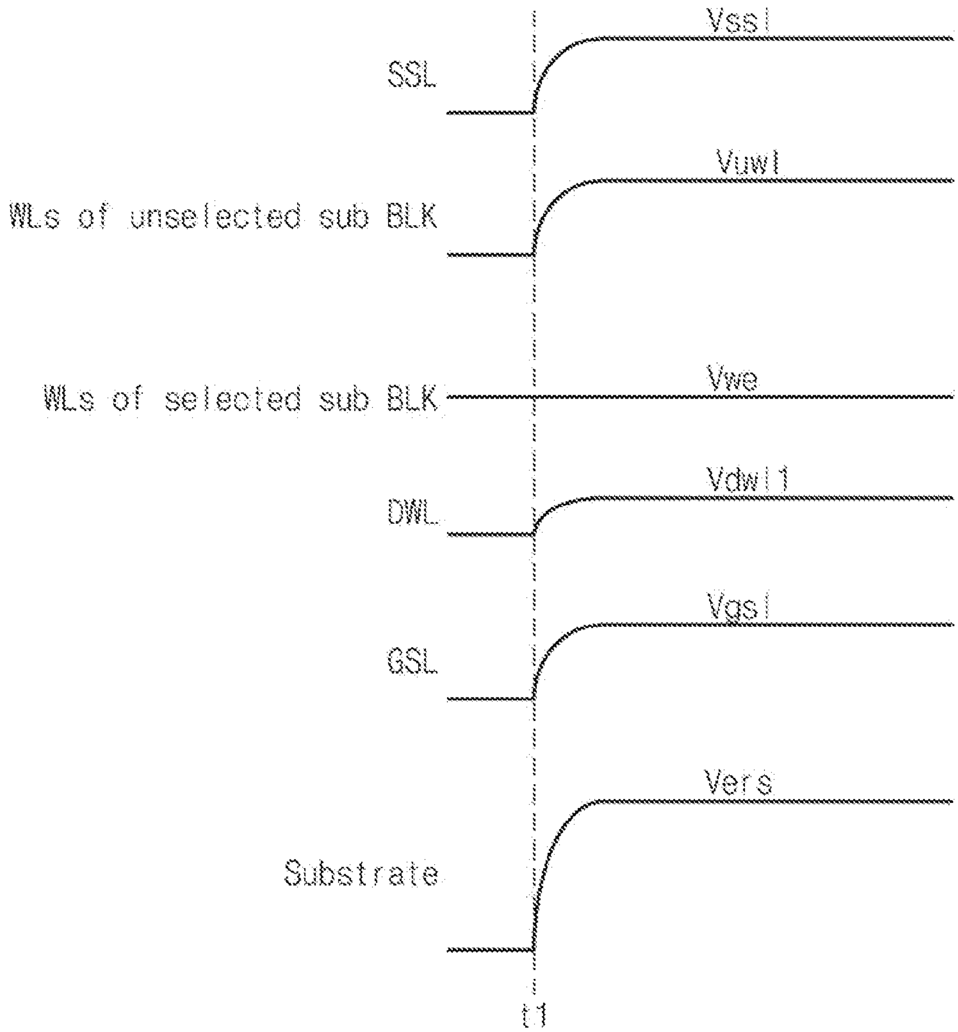
CSL
BL1
BL2
BL3
2nd Sub-block
1st Sub-block
SST
MC6
MC5
MC4
DMC
MC3
MC2
MC1
GST

Fig. 9

SSL	Float
WLs of unselected sub block	Float
WLs of selected sub block	Vwe
DWL	Vdwl1
GSL	Float
Substrate	Vers

Fig. 10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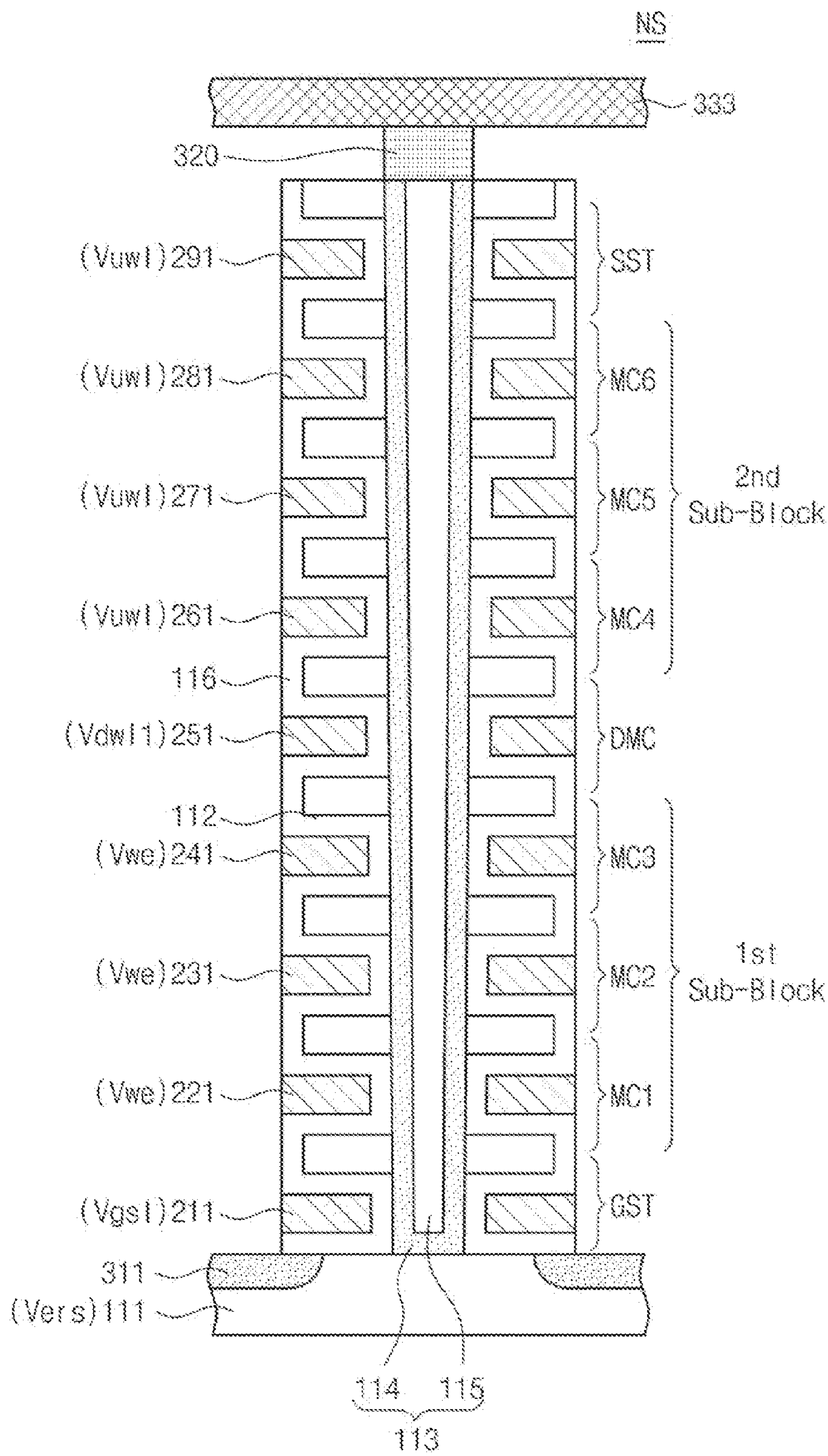
SSL
Vuwl
WLs of unselected sub BLK
Vwe
WLs of selected sub BLK
Vdwl1
DWL
Vgsl
GSL
Vers
Substrate
t1

Fig. 11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MC4
116
(Vdwl1)251
DMC
112
(Vwe)241
MC3
(Vwe)231
MC2
1st
Sub-Block
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MC1
(Vgsl)211
GST
311
(Vers)111
114
115
113

Fig. 12

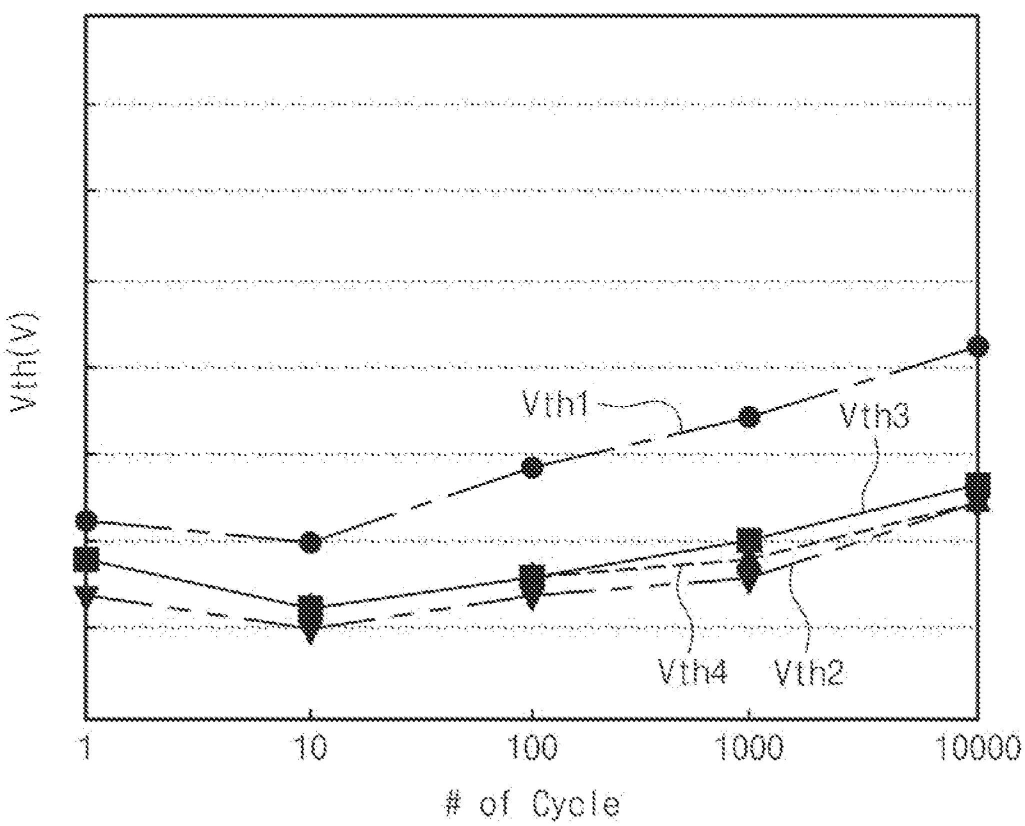


Fig. 13

SSL	Float
WLs of unselected sub block	Vwei
WLs of selected sub block	Vwe
DWL	Vdwl2
GSL	Float
Substrate	Vers

Fig. 14

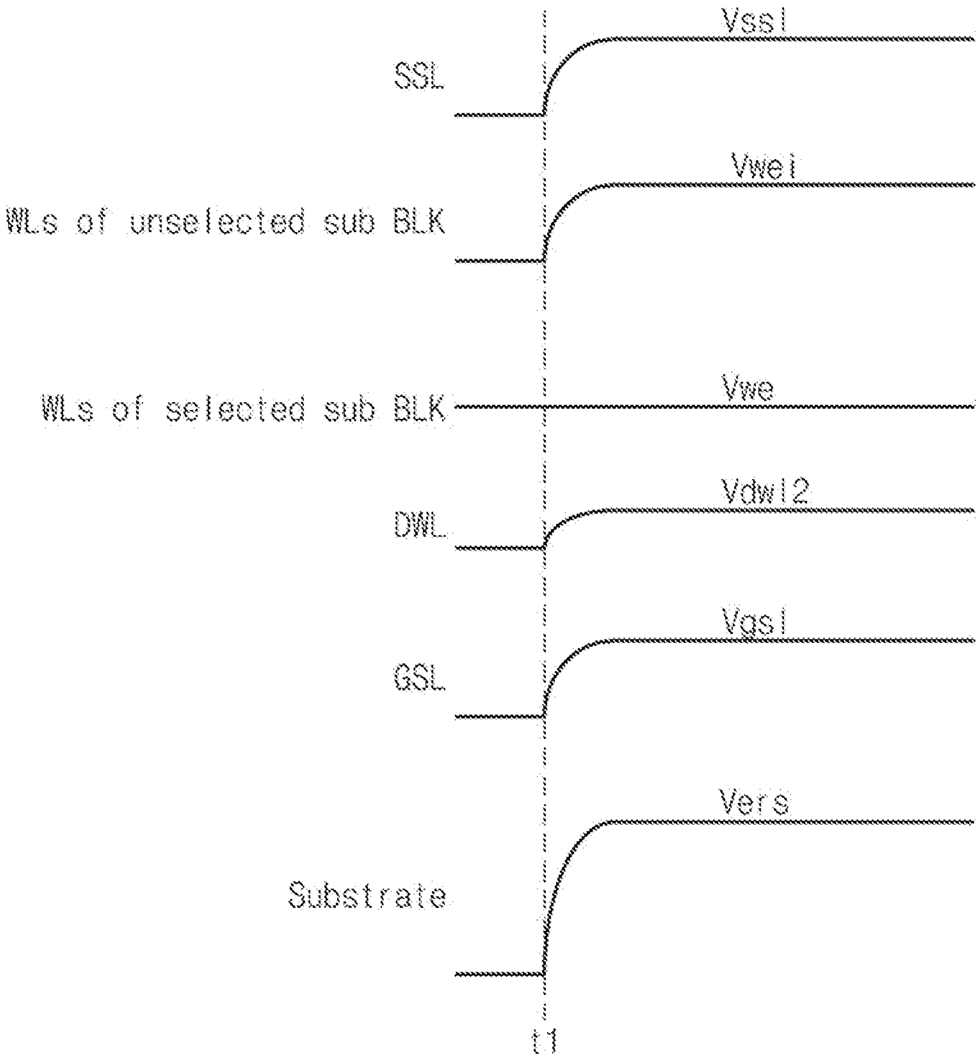

SSL
Vssl
WLs of unselected sub BLK
Vwei
WLs of selected sub BLK
Vwe
DWL
Vdwl2
GSL
Vgsl
Substrate
Vers
t1

Fig. 15

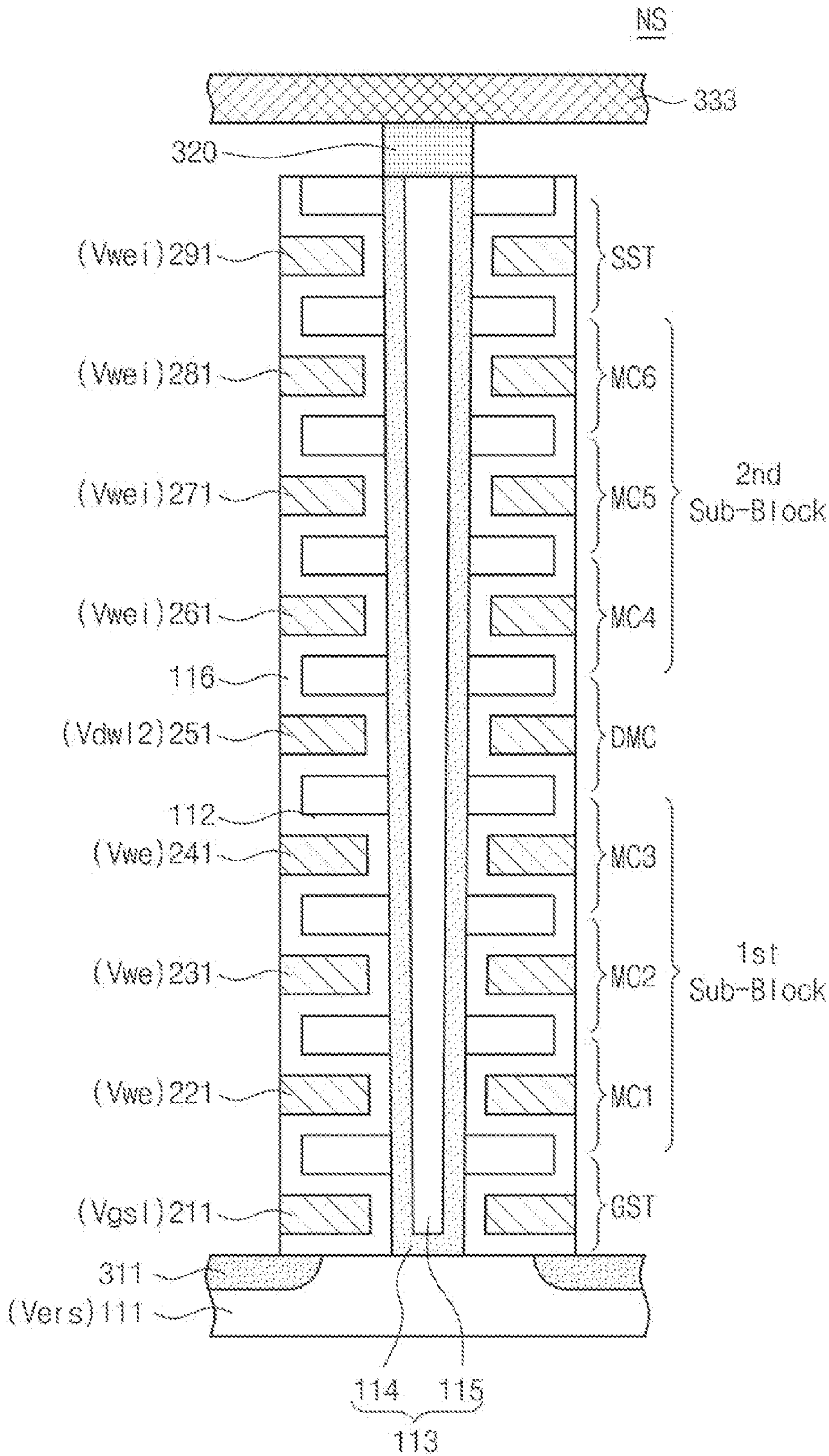
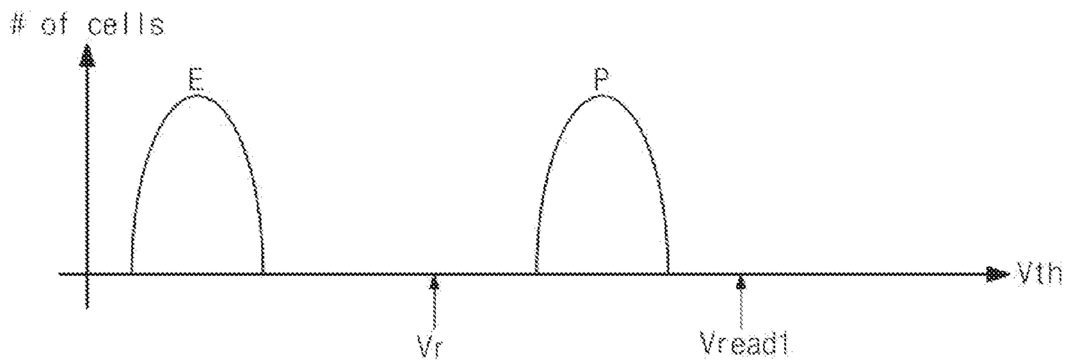
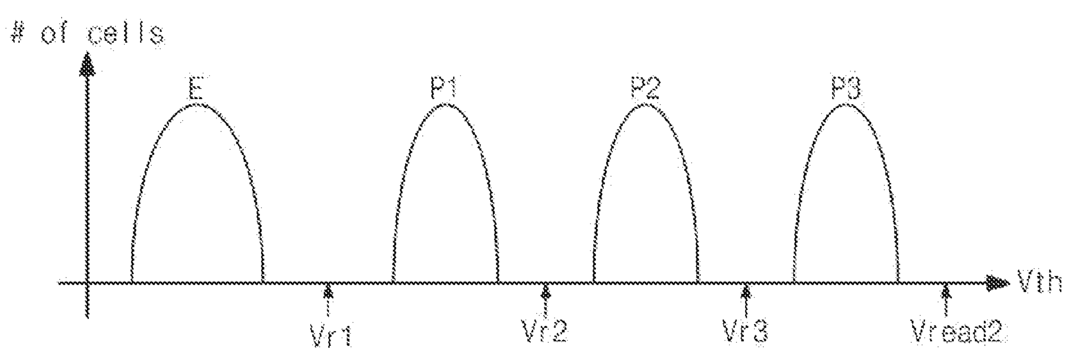

NS
333
320
(Vwei)291
(Vwei)281
(Vwei)271
(Vwei)261
116
(Vdwl2)251
112
(Vwe)241
(Vwe)231
(Vwe)221
(Vgsl)211
311
(Vers)111
114
115
113
SST
MC6
MC5
MC4
DMC
MC3
MC2
MC1
GST
2nd Sub-Block
1st Sub-Block

Fig. 16



# of cells
E
P
Vth
Vr
Vread1

Fig. 17



# of cells
E
P1
P2
P3
Vth
Vr1
Vr2
Vr3
Vread2

Fig. 18

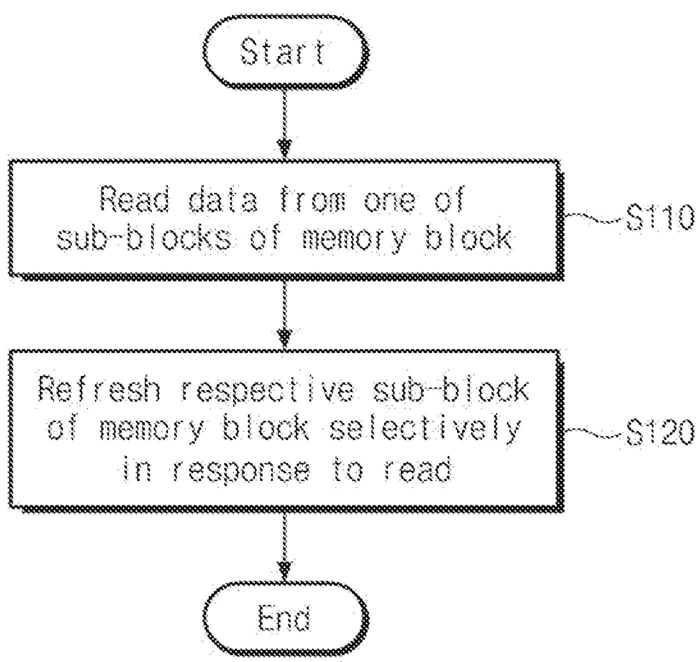

Start
Read data from one of sub-blocks of memory block
S110
Refresh respective sub-block of memory block selectively in response to read
S120
End

Fig. 19

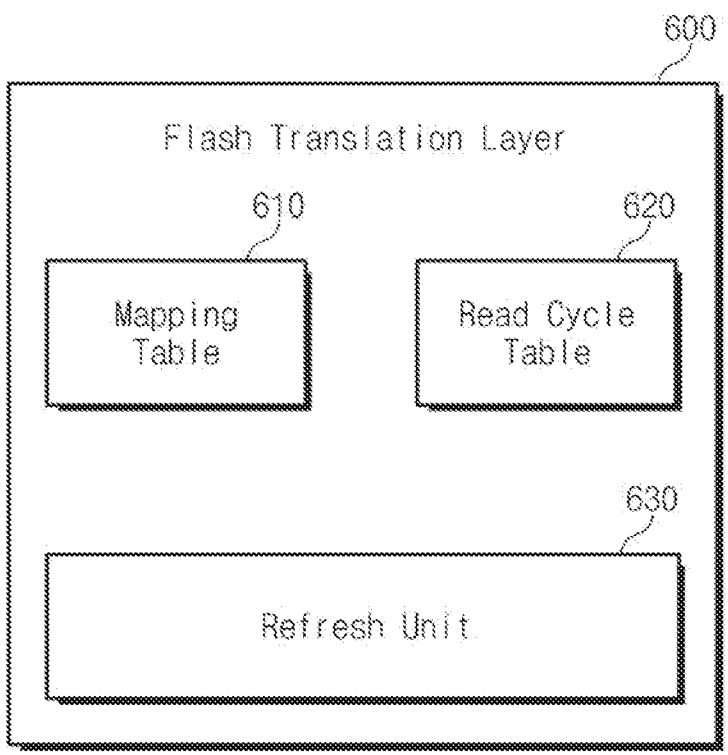

600
Flash Translation Layer
610
Mapping Table
620
Read Cycle Table
630
Refresh Unit

Fig. 20

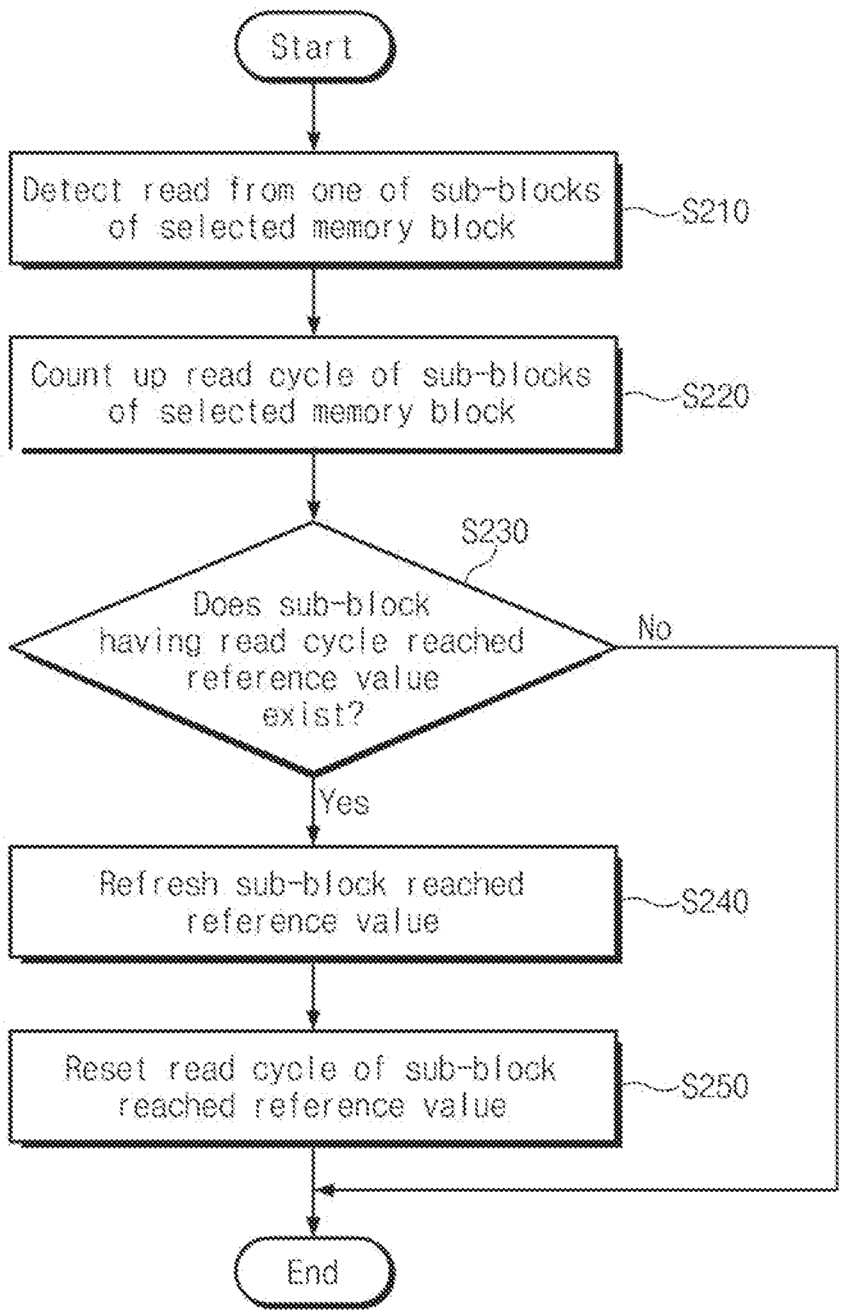

Start
Detect read from one of sub-blocks of selected memory block
S210
Count up read cycle of sub-blocks of selected memory block
S220
S230
Does sub-block having read cycle reached reference value exist?
No
Yes
Refresh sub-block reached reference value
S240
Reset read cycle of sub-block reached reference value
S250
End

Fig. 21

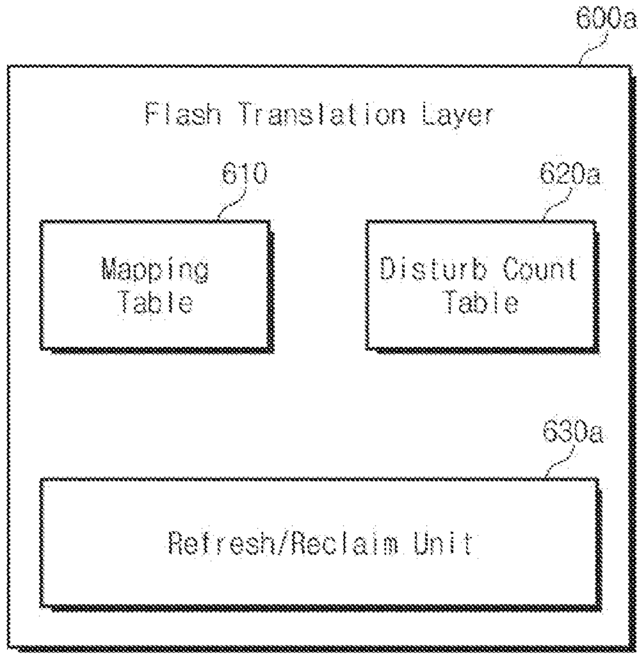

600a
Flash Translation Layer
610
Mapping Table
620a
Disturb Count Table
630a
Refresh/Reclaim Unit

Fig. 22

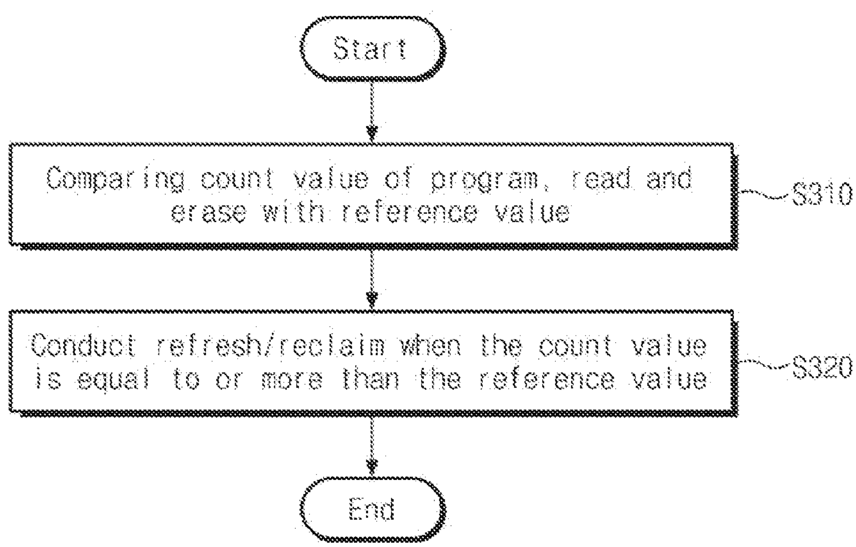

Start
Comparing count value of program, read and erase with reference value
S310
Conduct refresh/reclaim when the count value is equal to or more than the reference value
S320
End

Fig. 23

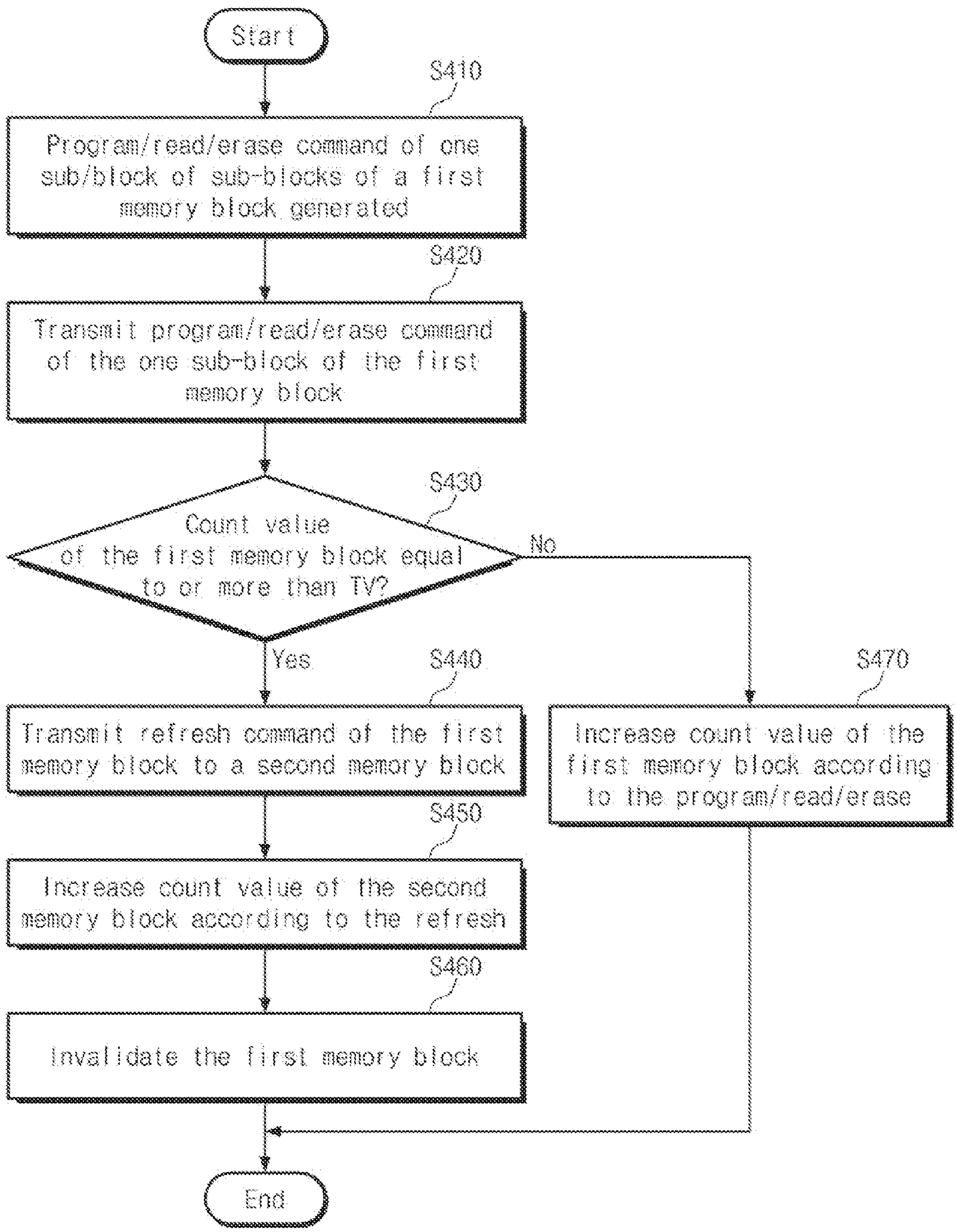

Start
S410
Program/read/erase command of one sub/block of sub-blocks of a first memory block generated
S420
Transmit program/read/erase command of the one sub-block of the first memory block
S430
Count value of the first memory block equal to or more than TV?
No
Yes
S440
Transmit refresh command of the first memory block to a second memory block
S450
Increase count value of the second memory block according to the refresh
S460
Invalidate the first memory block
S470
Increase count value of the first memory block according to the program/read/erase
End

Fig. 24

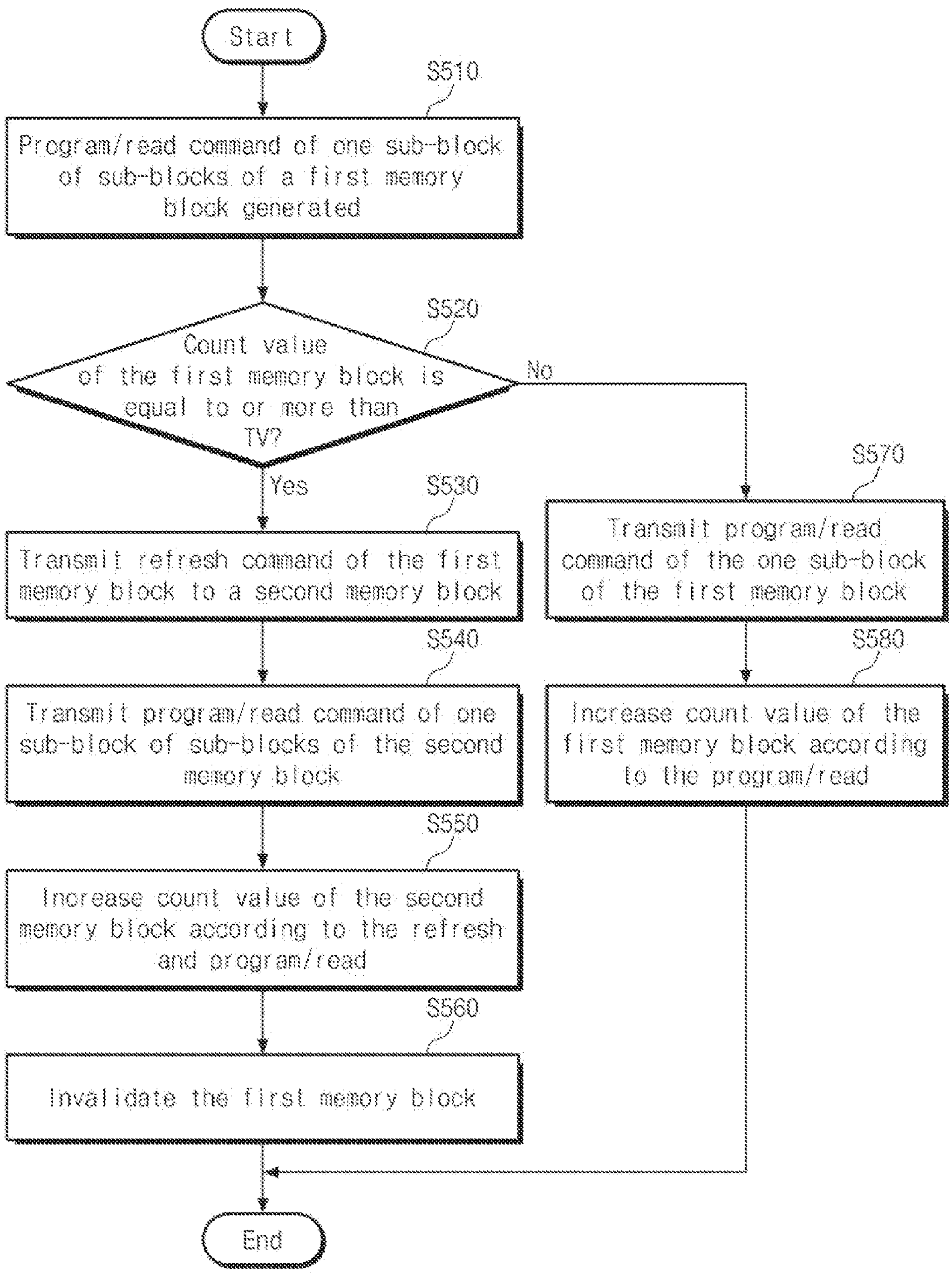

Start
S510
Program/read command of one sub-block of sub-blocks of a first memory block generated
S520
Count value of the first memory block is equal to or more than TV?
No
Yes
S530
Transmit refresh command of the first memory block to a second memory block
S540
Transmit program/read command of one sub-block of sub-blocks of the second memory block
S550
Increase count value of the second memory block according to the refresh and program/read
S560
Invalidate the first memory block
S570
Transmit program/read command of the one sub-block of the first memory block
S580
Increase count value of the first memory block according to the program/read
End

Fig. 25

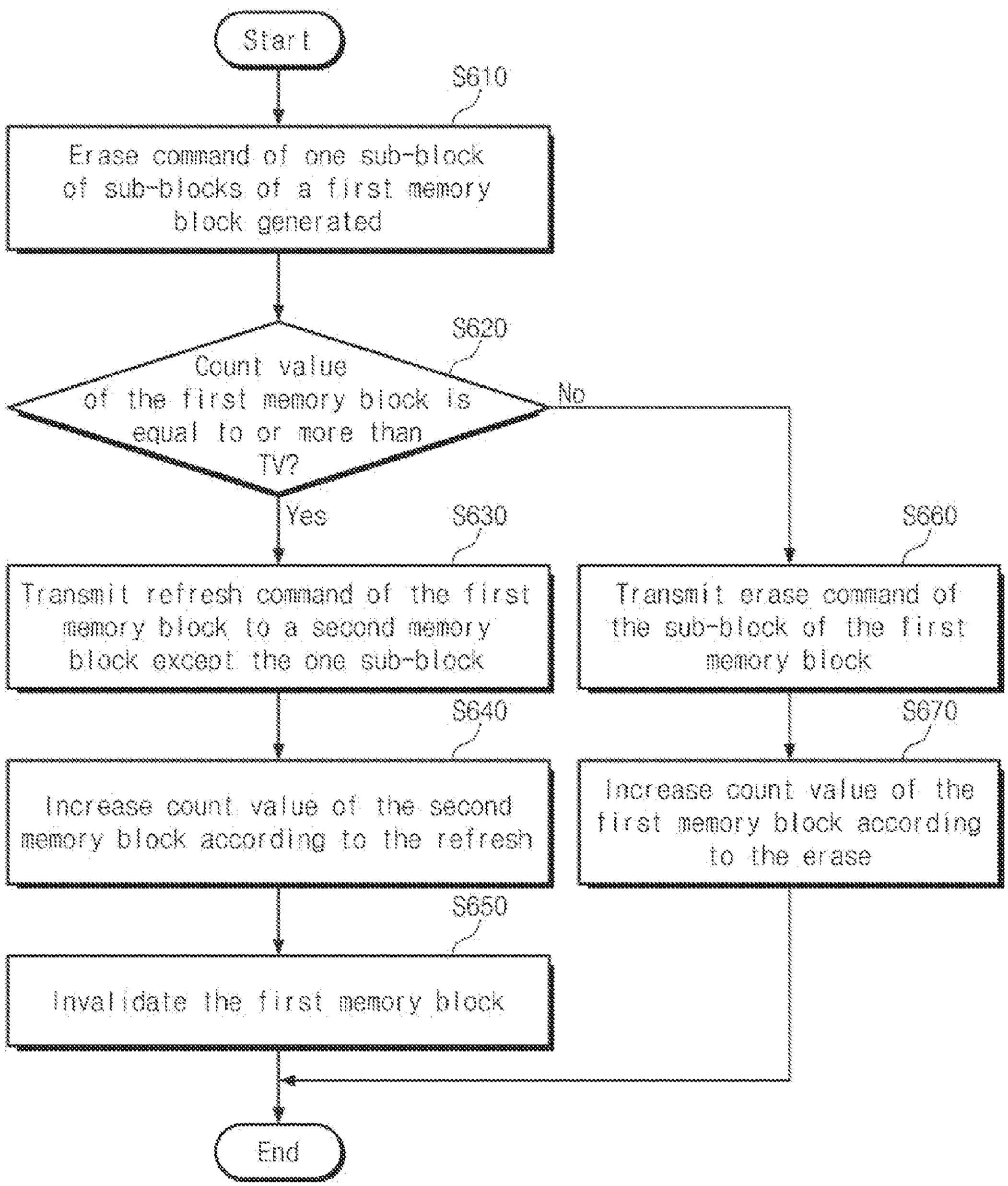

Start
S610
Erase command of one sub-block of sub-blocks of a first memory block generated
S620
Count value of the first memory block is equal to or more than TV?
No
Yes
S630
Transmit refresh command of the first memory block to a second memory block except the one sub-block
S660
Transmit erase command of the sub-block of the first memory block
S640
Increase count value of the second memory block according to the refresh
S670
Increase count value of the first memory block according to the erase
S650
Invalidate the first memory block
End

Fig. 26

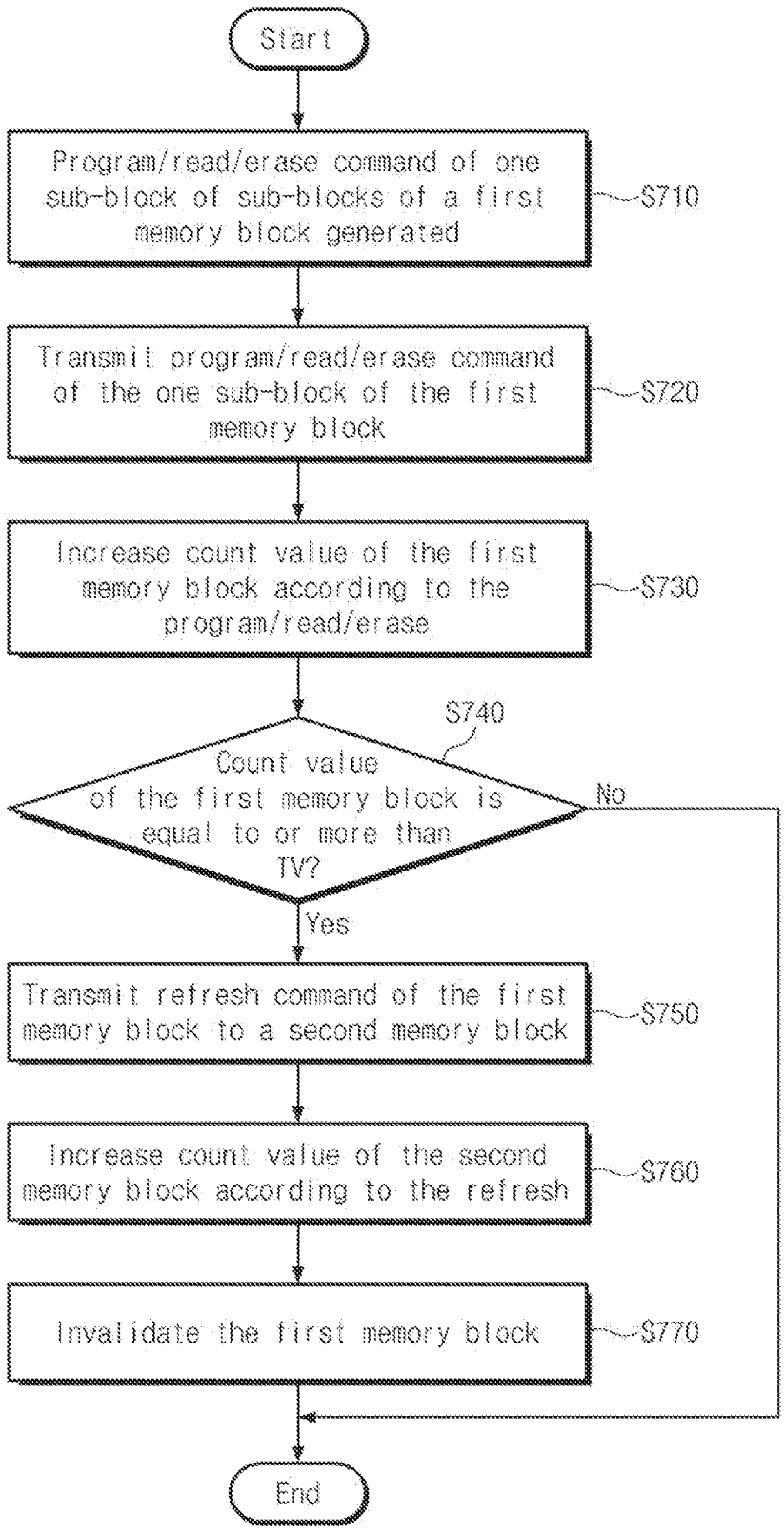

Start
Program/read/erase command of one sub-block of sub-blocks of a first memory block generated
S710
Transmit program/read/erase command of the one sub-block of the first memory block
S720
Increase count value of the first memory block according to the program/read/erase
S730
S740
Count value of the first memory block is equal to or more than TV?
No
Yes
Transmit refresh command of the first memory block to a second memory block
S750
Increase count value of the second memory block according to the refresh
S760
Invalidate the first memory block
S770
End

Fig. 27

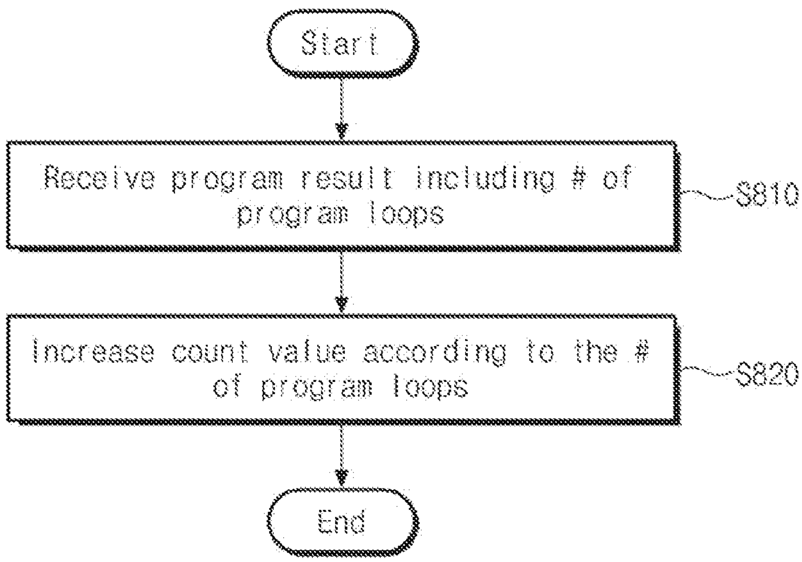

Start
Receive program result including # of program loops
S810
Increase count value according to the # of program loops
S820
End

Fig. 28

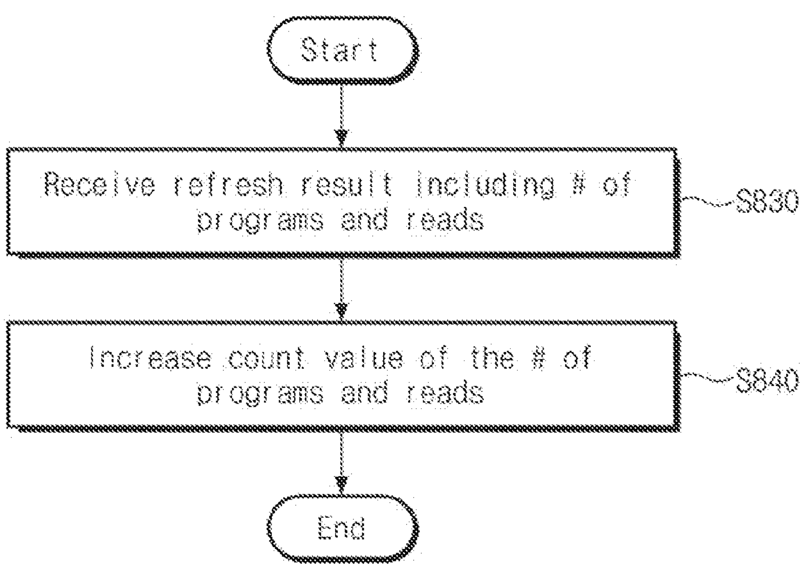
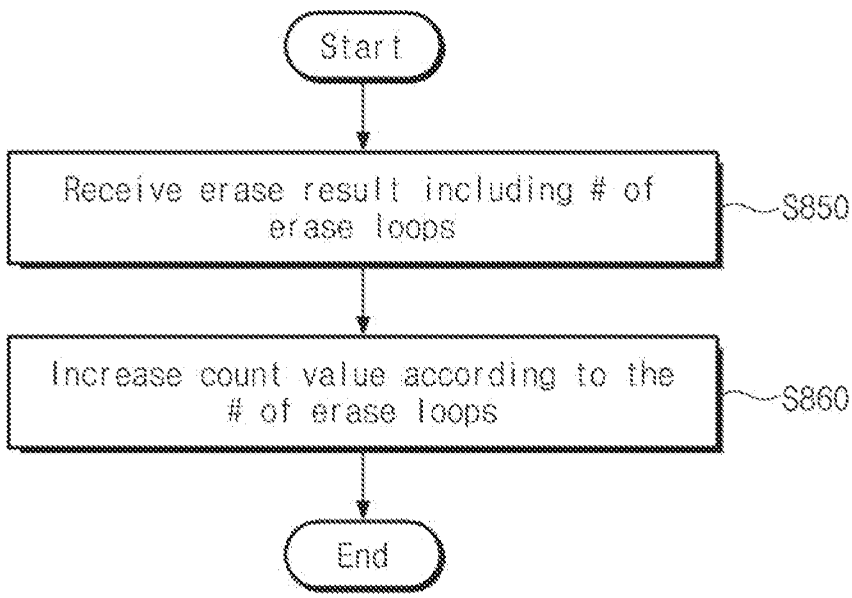

Start
Receive refresh result including # of programs and reads
S830
Increase count value of the # of programs and reads
S840
End

Fig. 29



Start
Receive erase result including # of erase loops
S850
Increase count value according to the # of erase loops
S860
End

Fig. 30

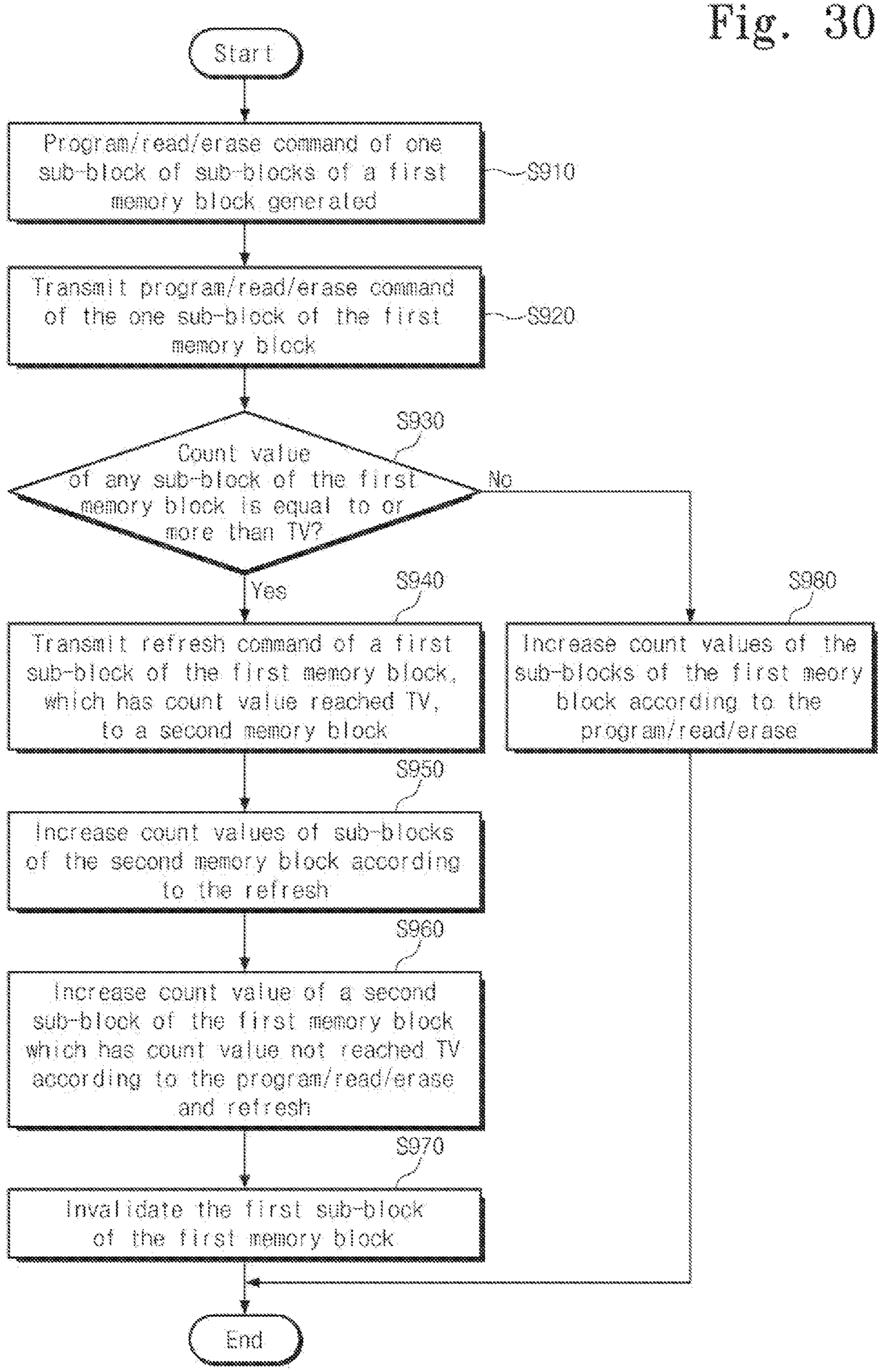

Start
Program/read/erase command of one sub-block of sub-blocks of a first memory block generated
S910
Transmit program/read/erase command of the one sub-block of the first memory block
S920
Count value of any sub-block of the first memory block is equal to or more than TV?
S930
No
Yes
Transmit refresh command of a first sub-block of the first memory block, which has count value reached TV, to a second memory block
S940
Increase count values of the sub-blocks of the first meory block according to the program/read/erase
S980
Increase count values of sub-blocks of the second memory block according to the refresh
S950
Increase count value of a second sub-block of the first memory block which has count value not reached TV according to the program/read/erase and refresh
S960
Invalidate the first sub-block of the first memory block
S970
End

Fig. 31

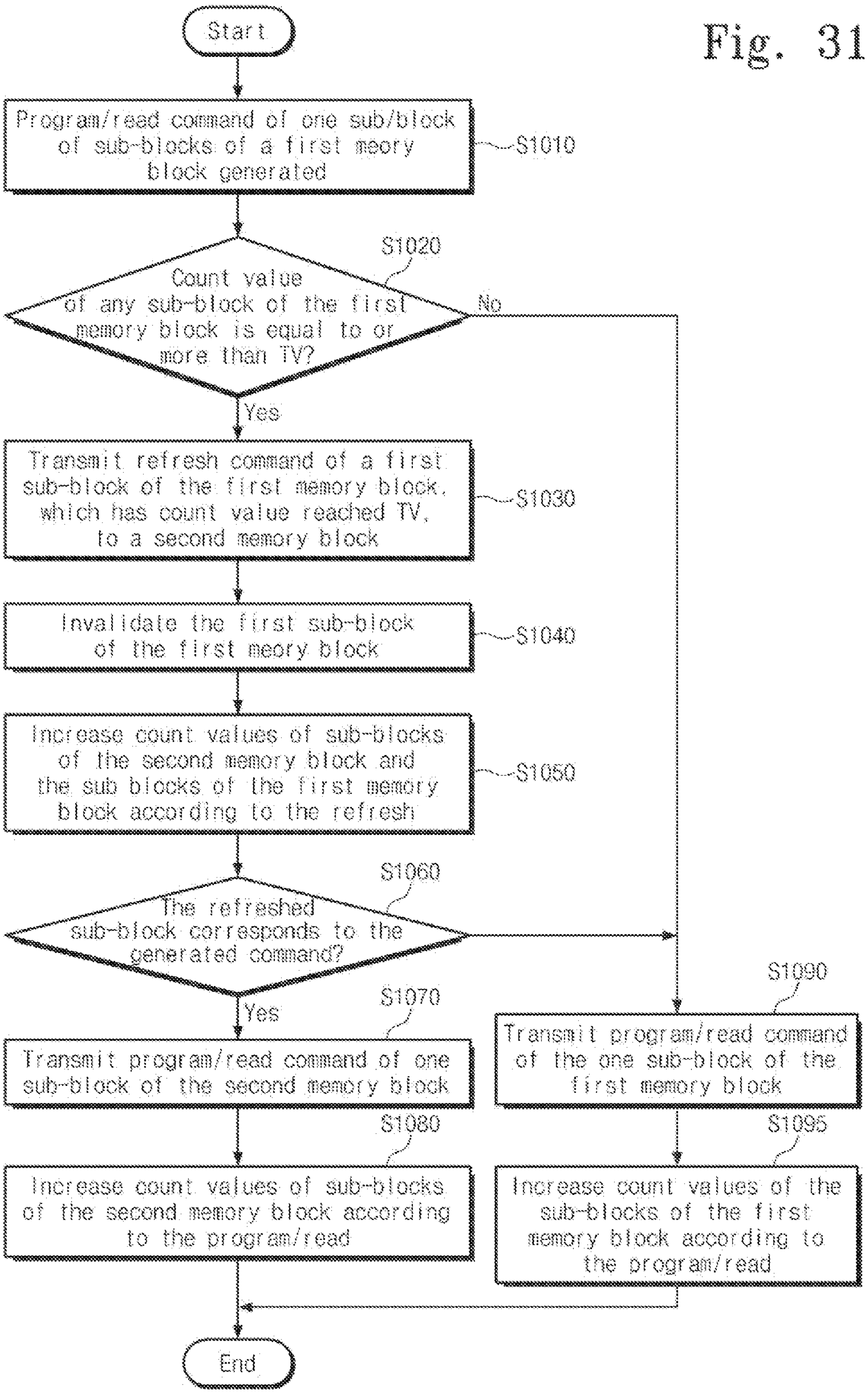

Start
Program/read command of one sub/block of sub-blocks of a first meory block generated
S1010
S1020
Count value of any sub-block of the first memory block is equal to or more than TV?
No
Yes
Transmit refresh command of a first sub-block of the first memory block, which has count value reached TV, to a second memory block
S1030
Invalidate the first sub-block of the first meory block
S1040
Increase count values of sub-blocks of the second memory block and the sub blocks of the first memory block according to the refresh
S1050
S1060
The refreshed sub-block corresponds to the generated command?
Yes
S1070
Transmit program/read command of one sub-block of the second memory block
S1080
Increase count values of sub-blocks of the second memory block according to the program/read
S1090
Transmit program/read command of the one sub-block of the first memory block
S1095
Increase count values of the sub-blocks of the first memory block according to the program/read
End

Fig. 32

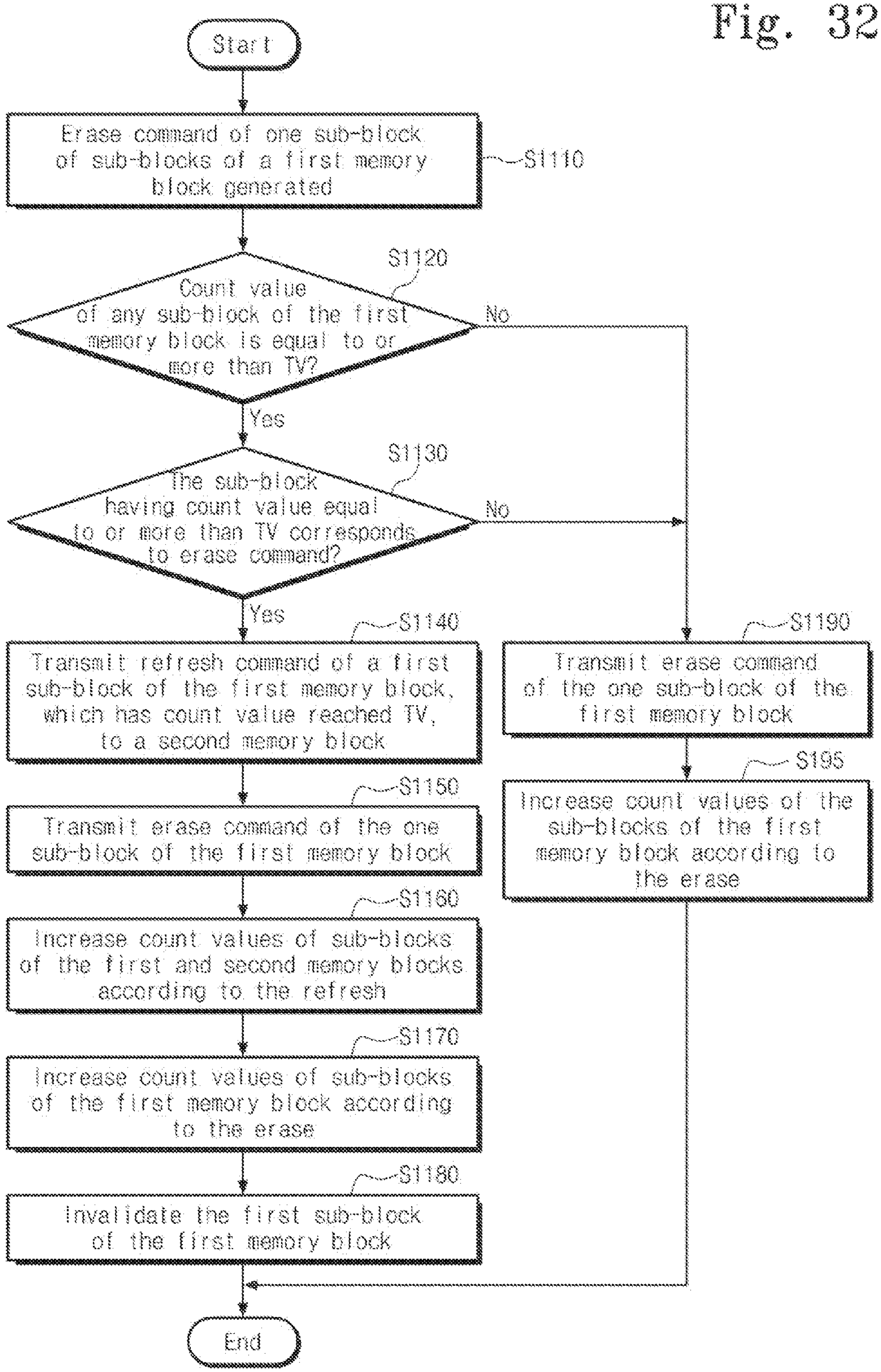

Start
Erase command of one sub-block of sub-blocks of a first memory block generated
S1110
S1120
Count value of any sub-block of the first memory block is equal to or more than TV?
No
Yes
S1130
The sub-block having count value equal to or more than TV corresponds to erase command?
No
Yes
S1140
Transmit refresh command of a first sub-block of the first memory block, which has count value reached TV, to a second memory block
S1150
Transmit erase command of the one sub-block of the first memory block
S1160
Increase count values of sub-blocks of the first and second memory blocks according to the refresh
S1170
Increase count values of sub-blocks of the first memory block according to the erase
S1180
Invalidate the first sub-block of the first memory block
S1190
Transmit erase command of the one sub-block of the first memory block
S195
Increase count values of the sub-blocks of the first memory block according to the erase
End

Fig. 33

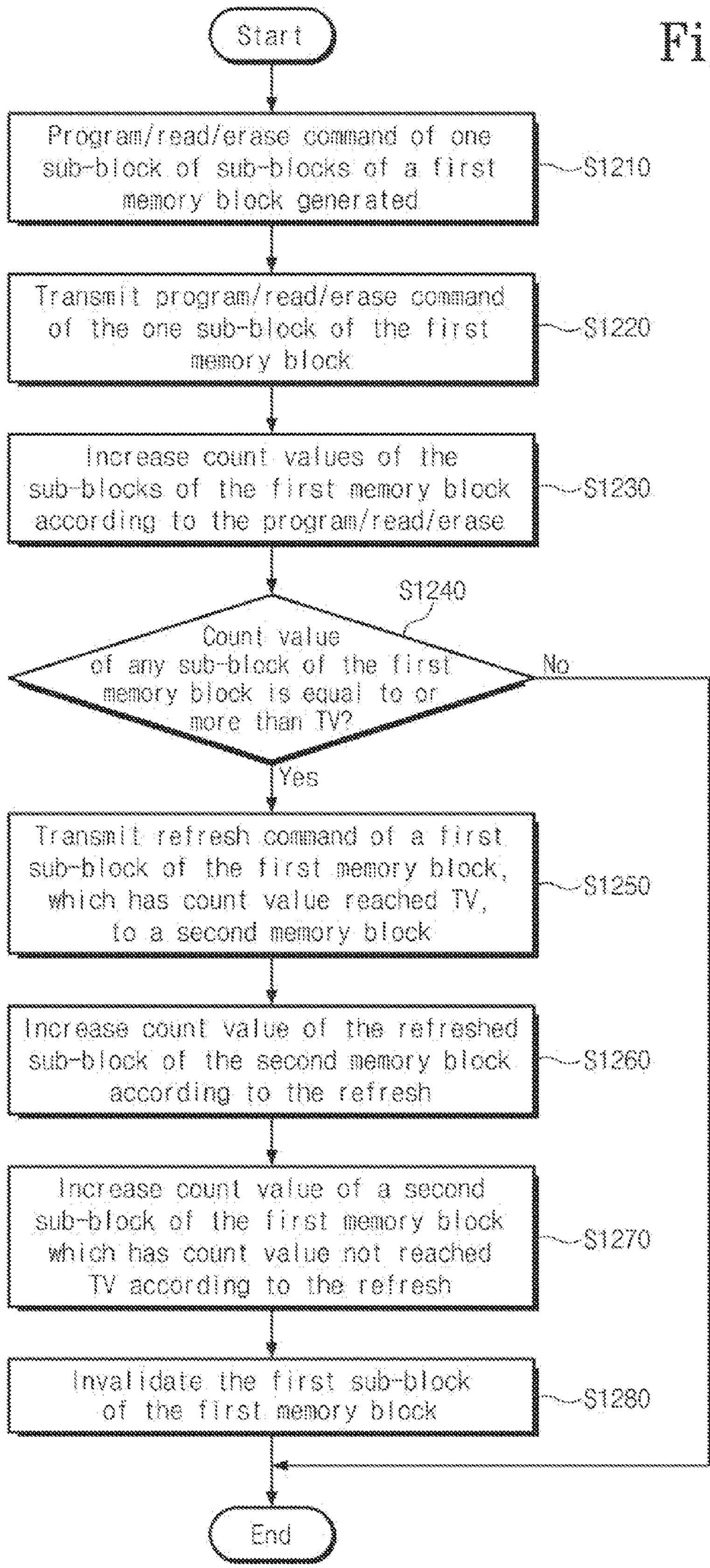

Start
Program/read/erase command of one sub-block of sub-blocks of a first memory block generated
S1210
Transmit program/read/erase command of the one sub-block of the first memory block
S1220
Increase count values of the sub-blocks of the first memory block according to the program/read/erase
S1230
S1240
Count value of any sub-block of the first memory block is equal to or more than TV?
No
Yes
Transmit refresh command of a first sub-block of the first memory block, which has count value reached TV, to a second memory block
S1250
Increase count value of the refreshed sub-block of the second memory block according to the refresh
S1260
Increase count value of a second sub-block of the first memory block which has count value not reached TV according to the refresh
S1270
Invalidate the first sub-block of the first memory block
S1280
End

Fig. 34

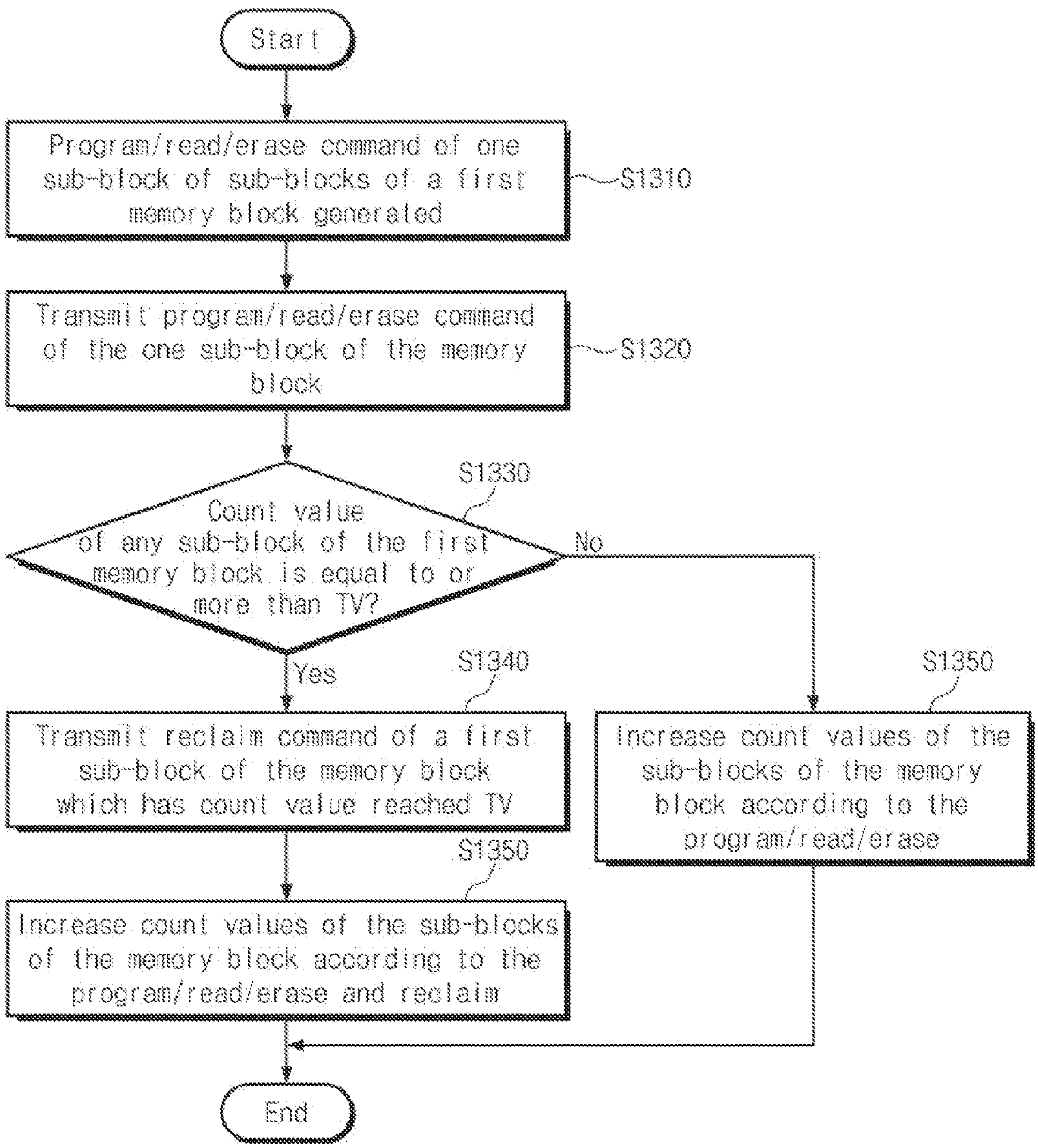

Start
Program/read/erase command of one sub-block of sub-blocks of a first memory block generated
S1310
Transmit program/read/erase command of the one sub-block of the memory block
S1320
S1330
Count value of any sub-block of the first memory block is equal to or more than TV?
No
Yes
S1340
Transmit reclaim command of a first sub-block of the memory block which has count value reached TV
S1350
Increase count values of the sub-blocks of the memory block according to the program/read/erase
S1350
Increase count values of the sub-blocks of the memory block according to the program/read/erase and reclaim
End

Fig. 35

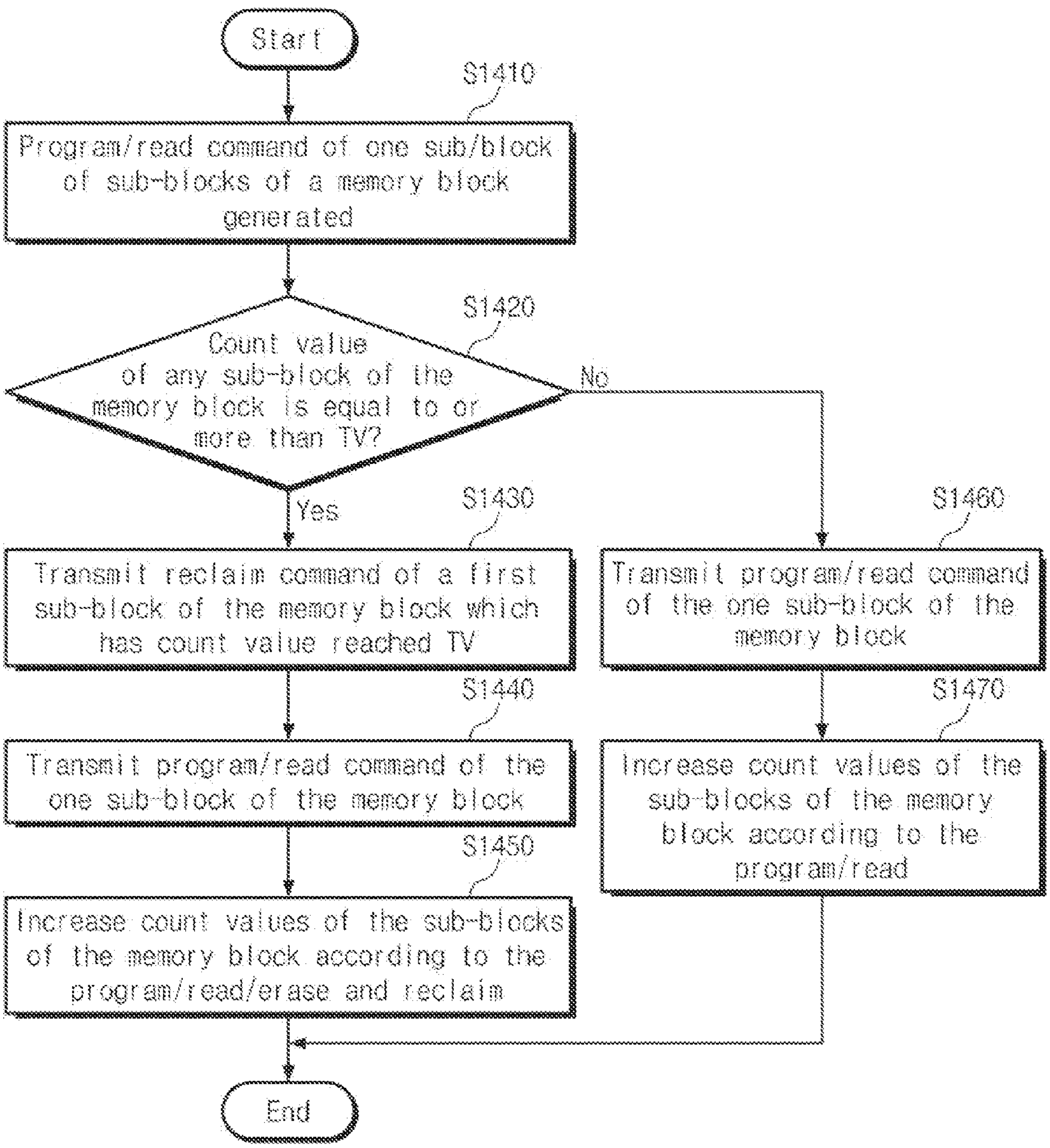

Start
S1410
Program/read command of one sub/block of sub-blocks of a memory block generated
S1420
Count value of any sub-block of the memory block is equal to or more than TV?
No
Yes
S1430
Transmit reclaim command of a first sub-block of the memory block which has count value reached TV
S1440
Transmit program/read command of the one sub-block of the memory block
S1450
Increase count values of the sub-blocks of the memory block according to the program/read/erase and reclaim
S1460
Transmit program/read command of the one sub-block of the memory block
S1470
Increase count values of the sub-blocks of the memory block according to the program/read
End

Fig. 36

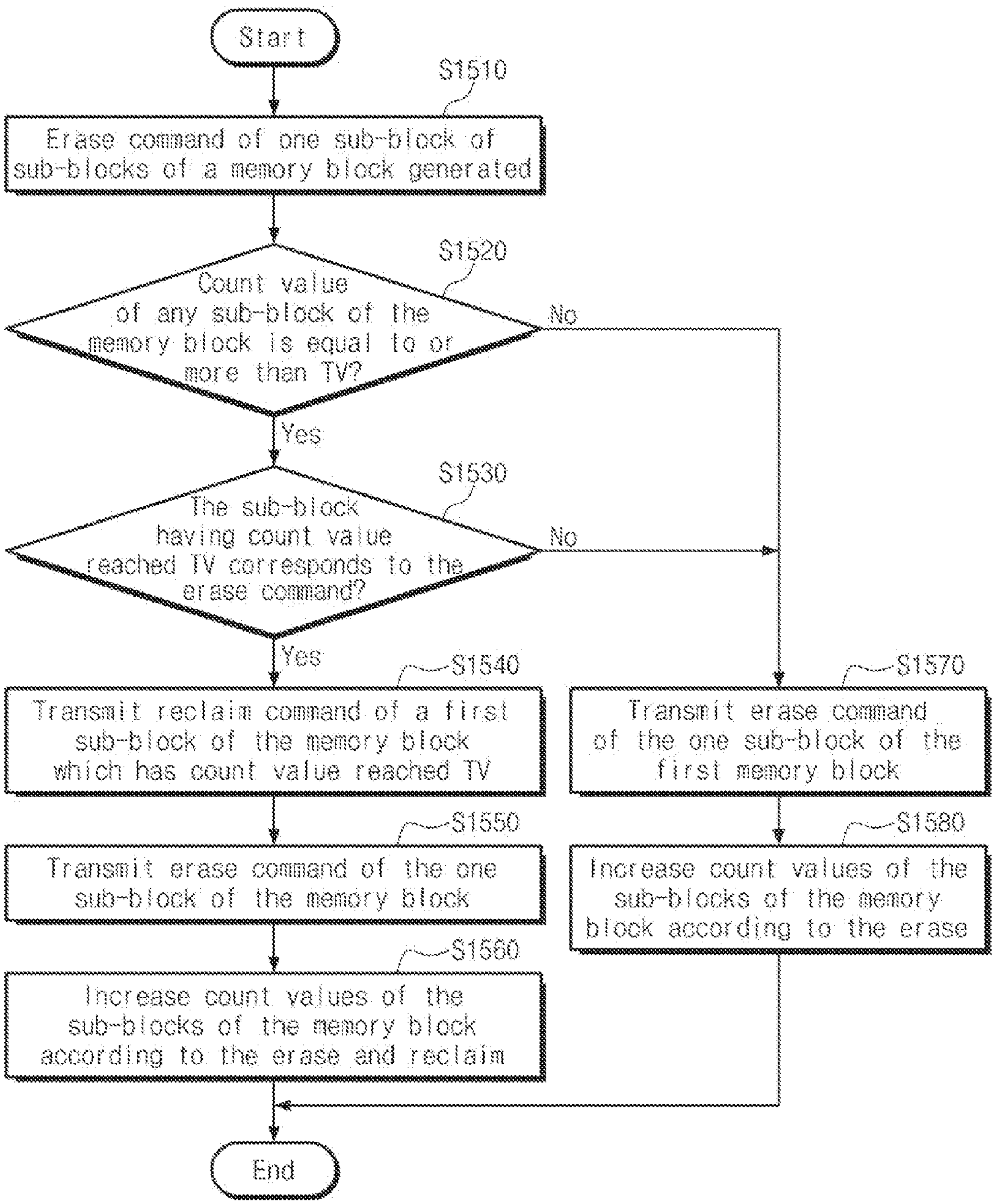
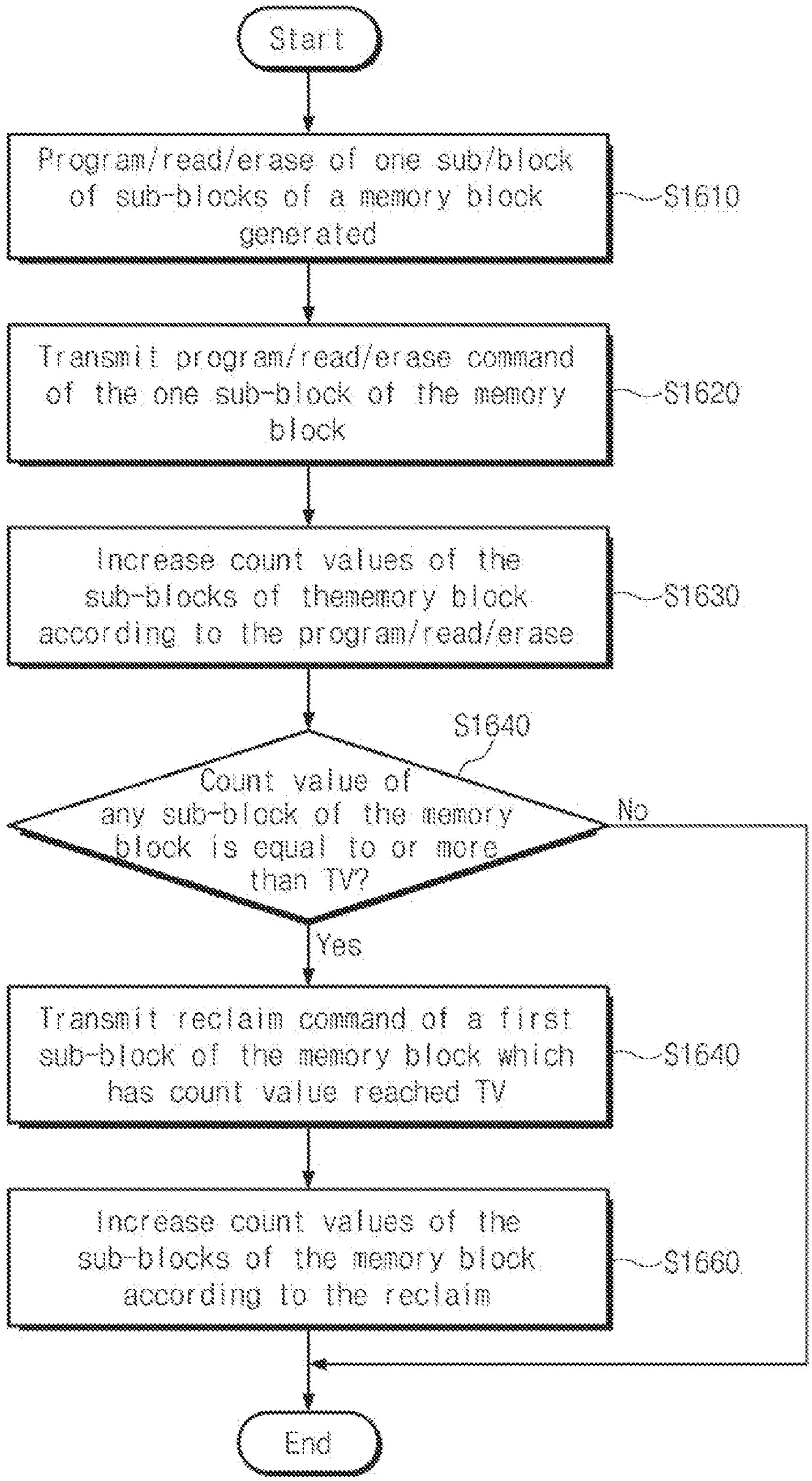

Start
S1510
Erase command of one sub-block of sub-blocks of a memory block generated
S1520
Count value of any sub-block of the memory block is equal to or more than TV?
No
Yes
S1530
The sub-block having count value reached TV corresponds to the erase command?
No
Yes
S1540
Transmit reclaim command of a first sub-block of the memory block which has count value reached TV
S1550
Transmit erase command of the one sub-block of the memory block
S1560
Increase count values of the sub-blocks of the memory block according to the erase and reclaim
S1570
Transmit erase command of the one sub-block of the first memory block
S1580
Increase count values of the sub-blocks of the memory block according to the erase
End

Fig. 37



Start
Program/read/erase of one sub/block of sub-blocks of a memory block generated
S1610
Transmit program/read/erase command of the one sub-block of the memory block
S1620
Increase count values of the sub-blocks of thememory block according to the program/read/erase
S1630
S1640
Count value of any sub-block of the memory block is equal to or more than TV?
No
Yes
Transmit reclaim command of a first sub-block of the memory block which has count value reached TV
S1640
Increase count values of the sub-blocks of the memory block according to the reclaim
S1660
End

Fig. 38

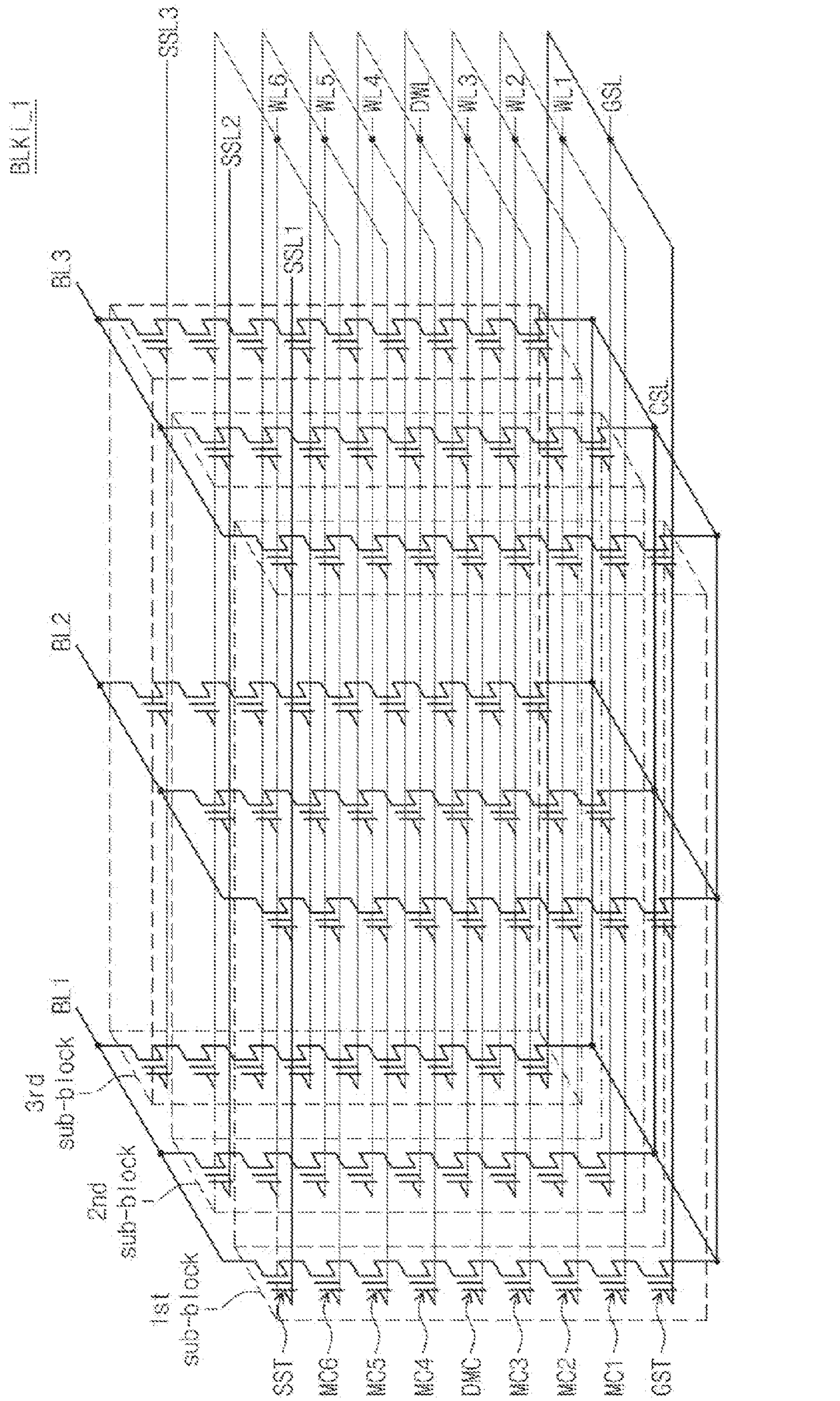

BLKi_1
SSL3
SSL2
SSL1
WL6
WL5
WL4
DWL
WL3
WL2
WL1
GSL
BL3
BL2
BL1
GSL
3rd sub-block
2nd sub-block
1st sub-block
SST
MC6
MC5
MC4
DMC
MC3
MC2
MC1
GST

Fig. 39

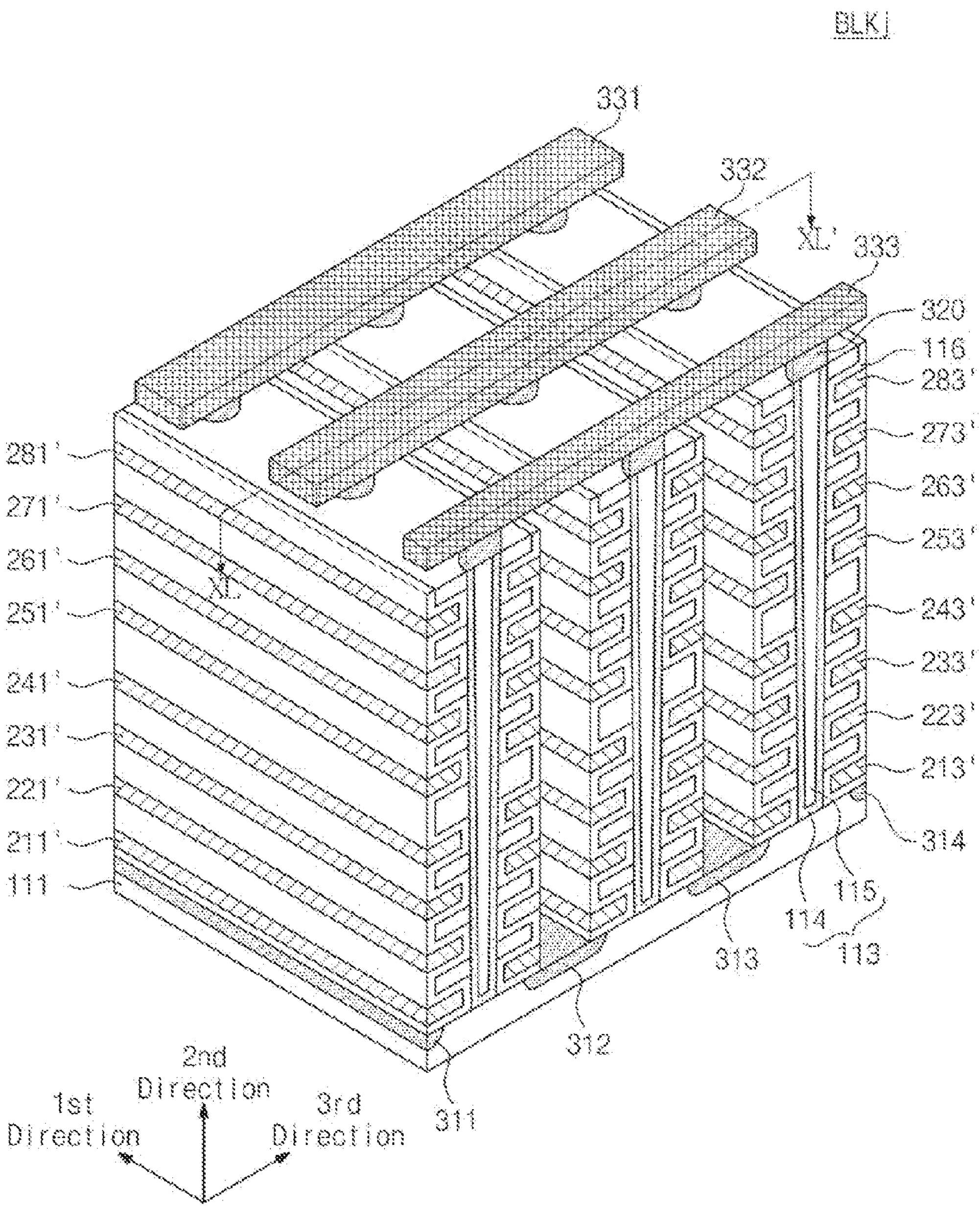

BLKj
331
332
XL'
333
320
116
283'
273'
263'
253'
243'
233'
223'
213'
314
115
114
113
313
312
311
281'
271'
261'
251'
241'
231'
221'
211'
111
XL
2nd Direction
1st Direction
3rd Direction

Fig. 40

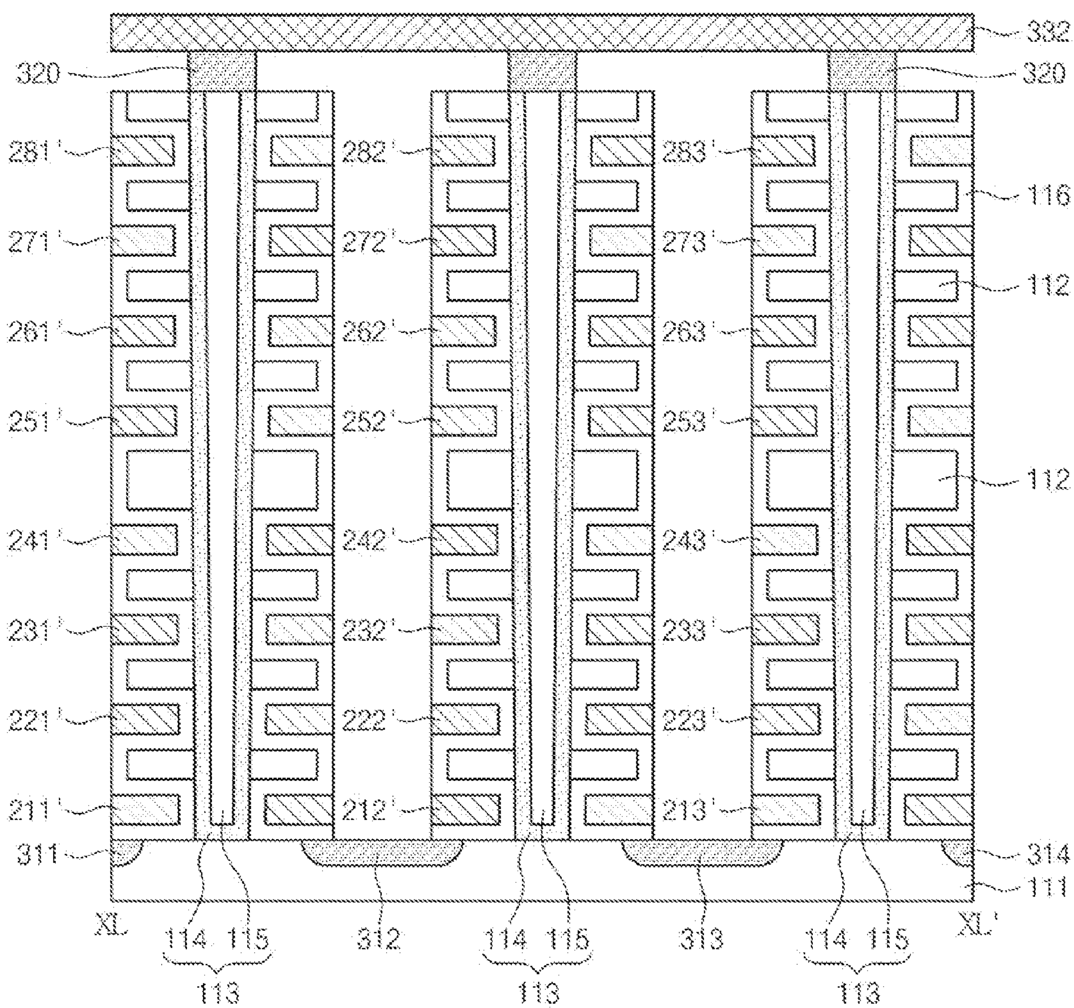

332
320
320
281'
282'
283'
116
271'
272'
273'
112
261'
262'
263'
251'
252'
253'
112'
241'
242'
243'
231'
232'
233'
221'
222'
223'
211'
212'
213'
311
314
111
XL
XL'
114 115
312
114 115
313
114 115
113
113
113

Fig. 41

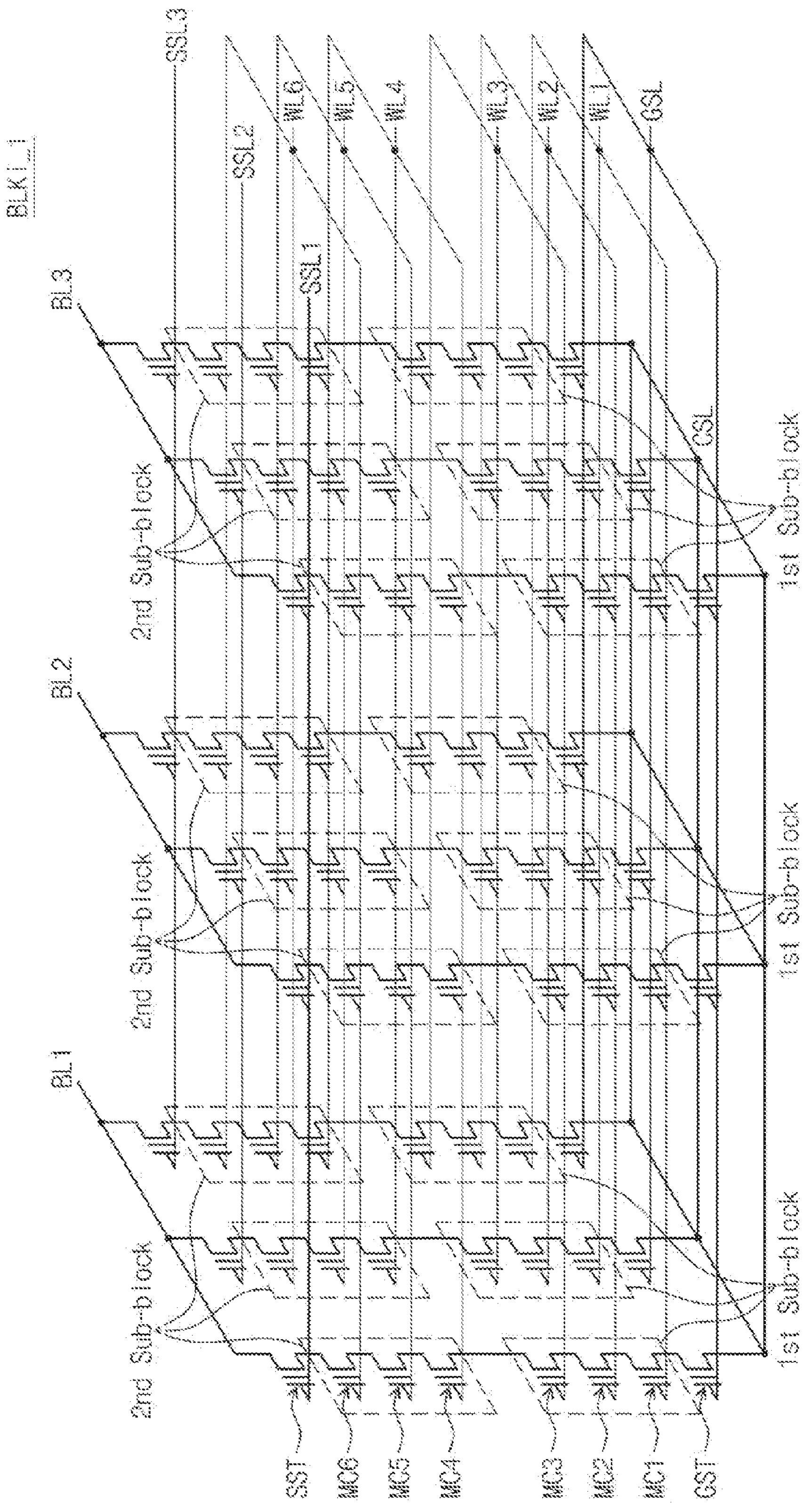

BLKi_1
SSL3
SSL2
SSL1
WL6
WL5
WL4
WL3
WL2
WL1
GSL
BL1
BL2
BL3
CSL
2nd Sub-block
2nd Sub-block
2nd Sub-block
1st Sub-block
1st Sub-block
1st Sub-block
SST
MC6
MC5
MC4
MC3
MC2
MC1
GST

Fig. 42

SSL	Float
WLs of unselected sub block	Float
WLs of selected sub block	Vwe
GSL	Float
Substrate	Vers

Fig. 43

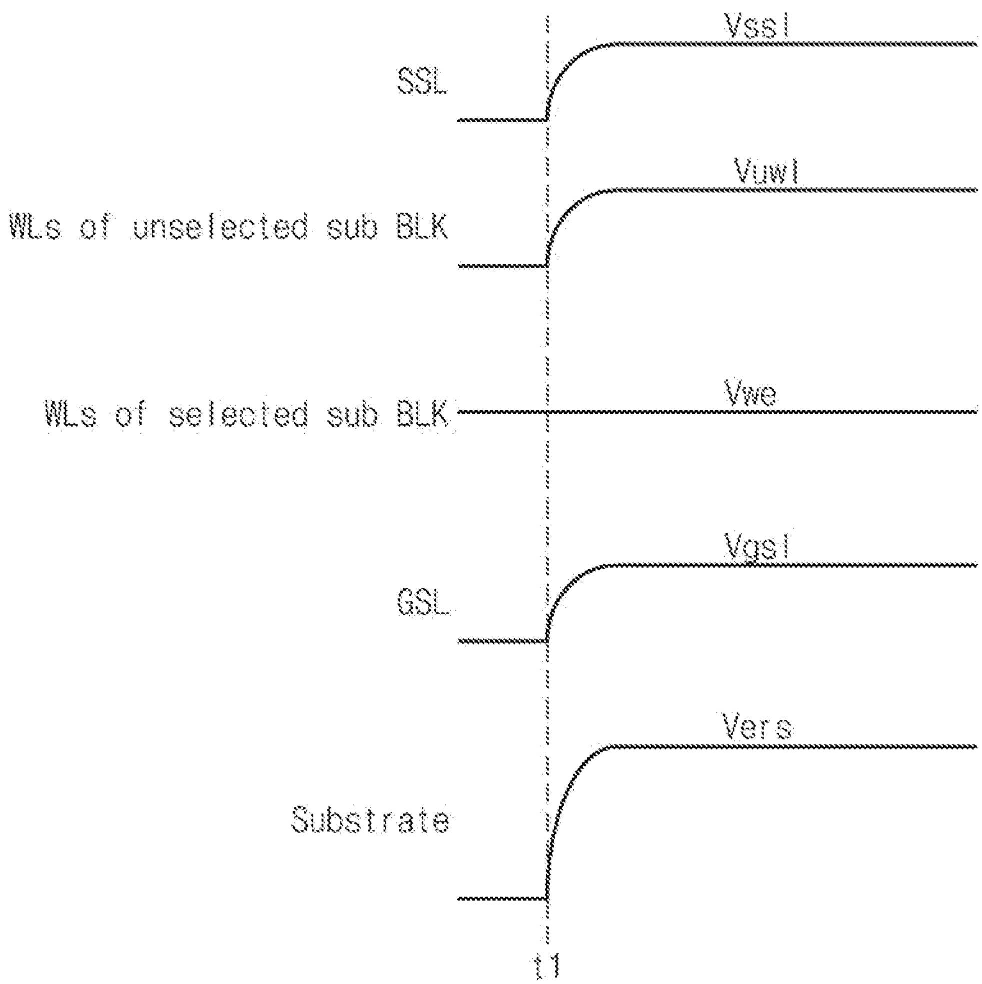

Vssl
SSL
Vuwl
WLs of unselected sub BLK
Vwe
WLs of selected sub BLK
Vgsl
GSL
Vers
Substrate
t1

Fig. 44

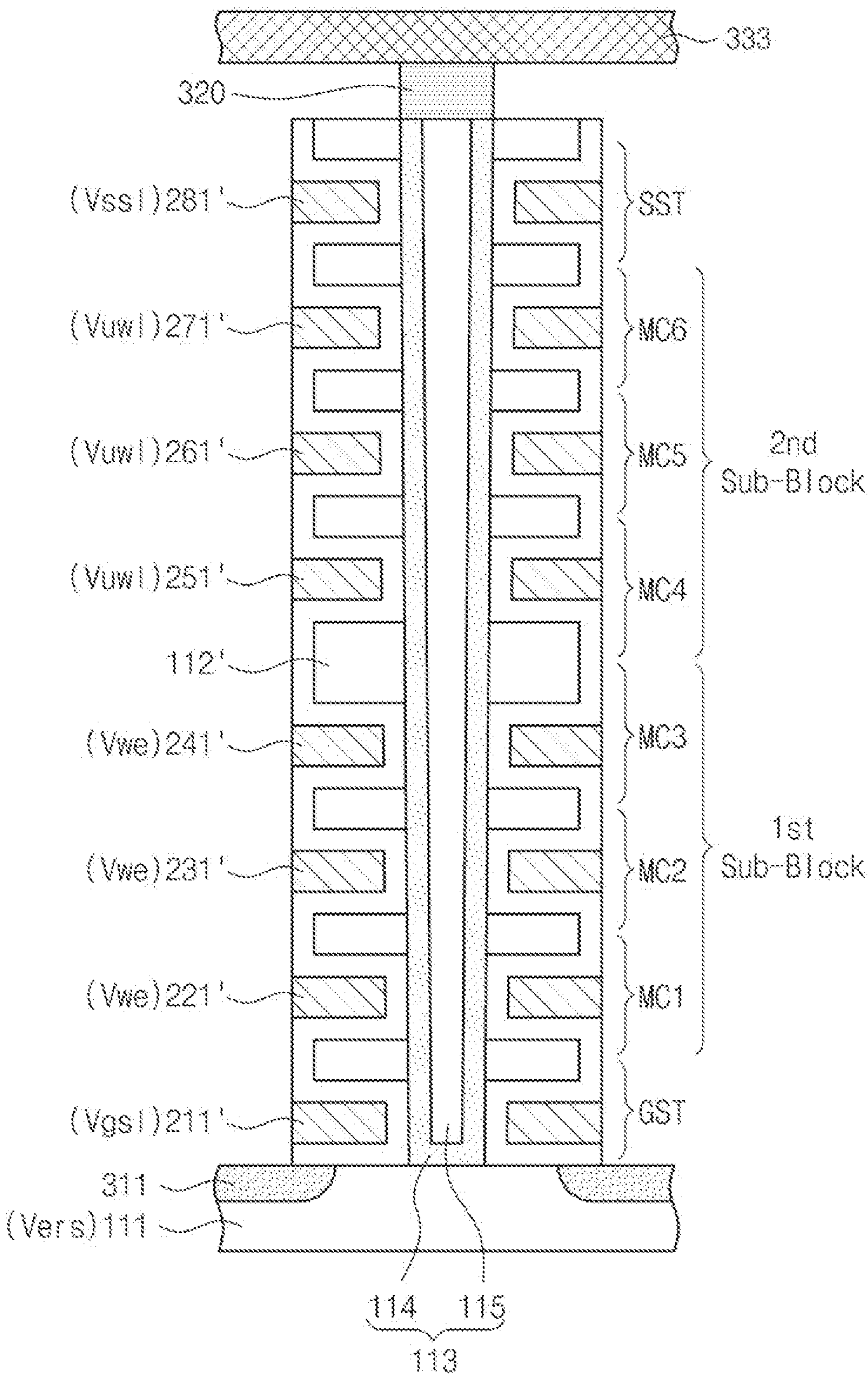

333
320
(Vssl)281'
SST
(Vuwl)271'
MC6
(Vuwl)261'
MC5
2nd
Sub-Block
(Vuwl)251'
MC4
112'
(Vwe)241'
MC3
(Vwe)231'
MC2
1st
Sub-Block
(Vwe)221'
MC1
(Vgsl)211'
GST
311
(Vers)111
114
115
113

Fig. 45

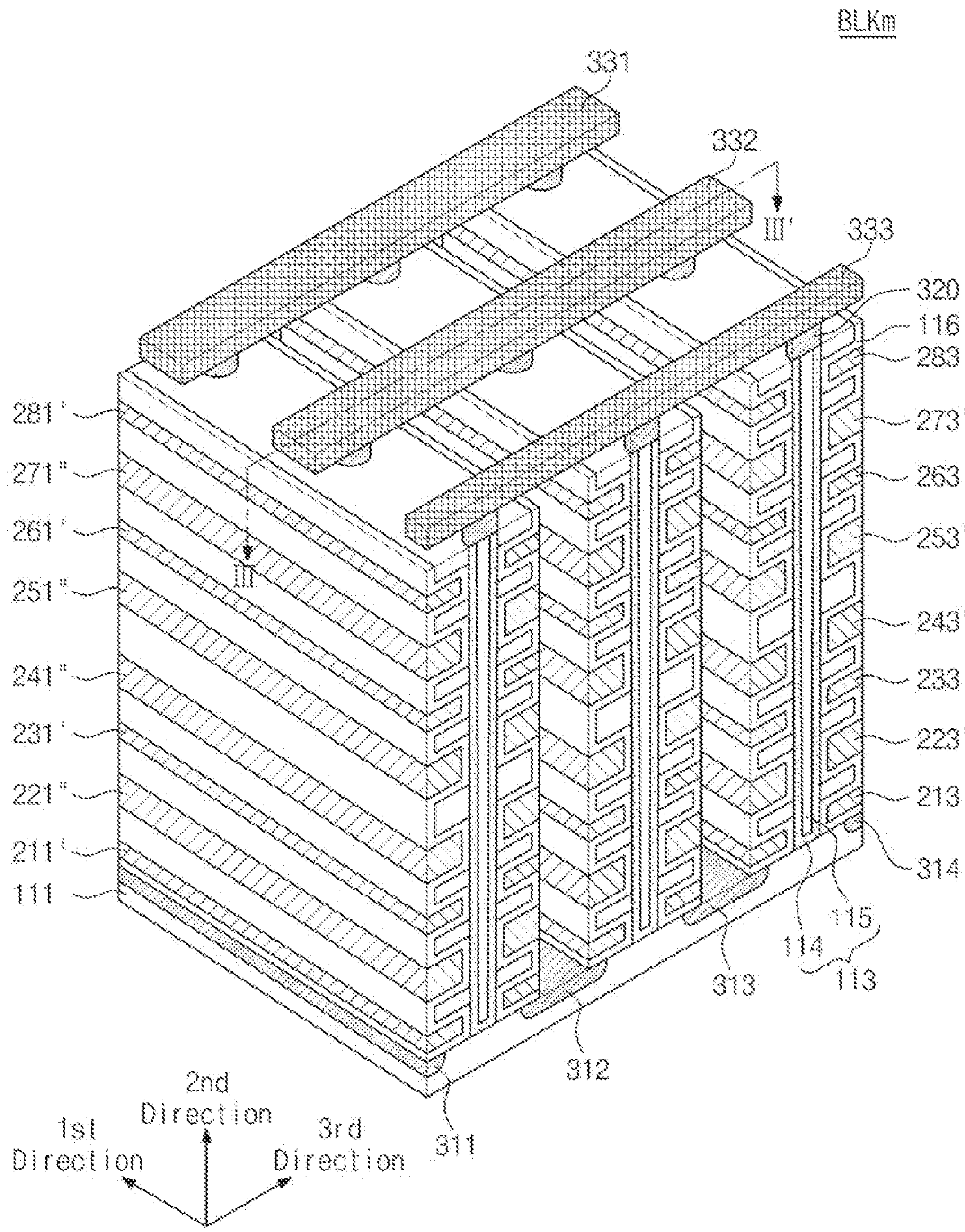

BLKm
331
332
III'
333
320
116
283'
273"
263'
253"
243"
233'
223"
213'
314
281'
271"
261'
251"
241"
231'
221"
211'
111
III
115
114
113
313
312
311
2nd Direction
1st Direction
3rd Direction

Fig. 46

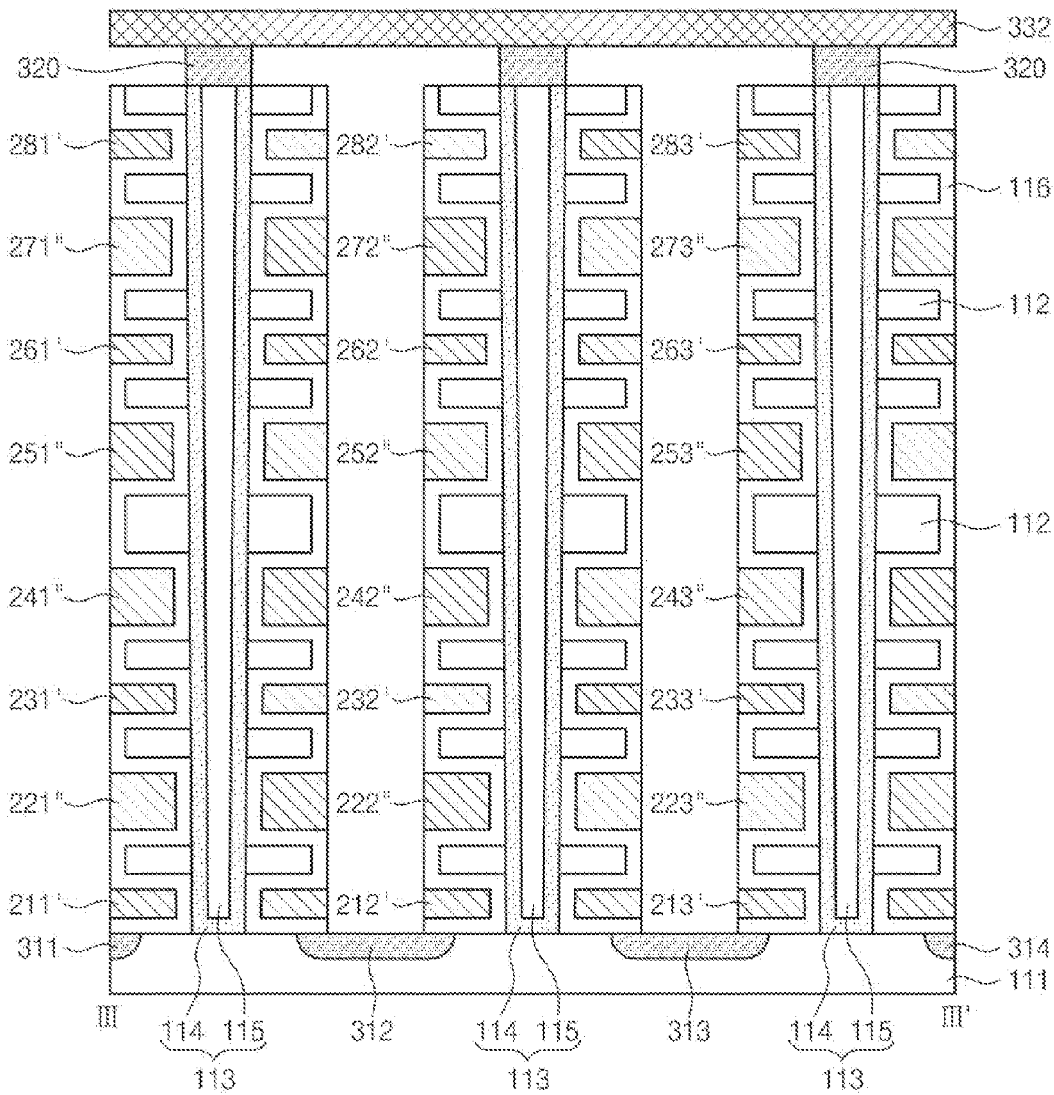
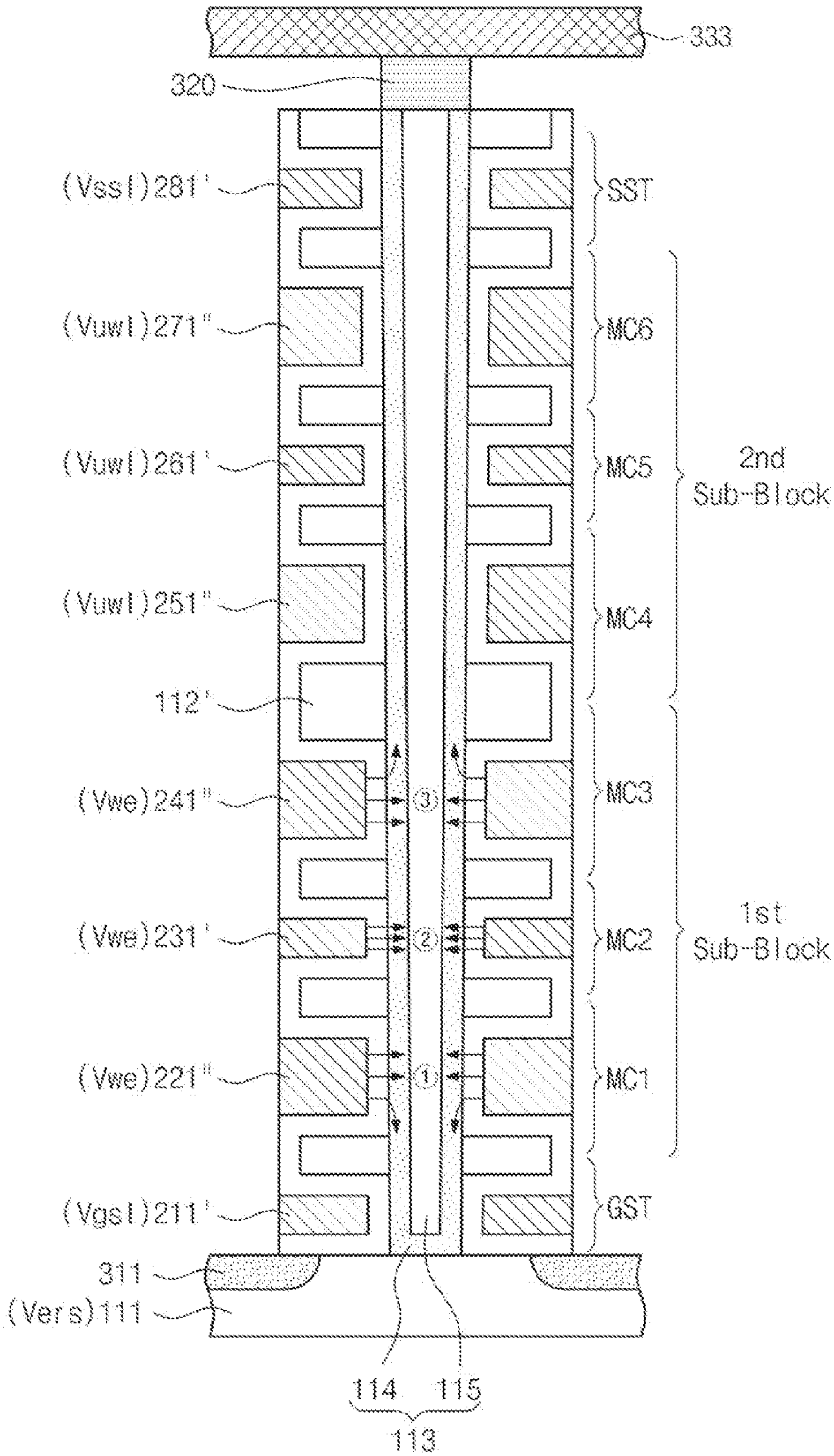

332
320
320
281'
282'
283'
116
271"
272"
273"
112
261'
262'
263'
251"
252"
253"
112'
241"
242"
243"
231'
232'
233'
221"
222"
223"
211'
212'
213'
311
314
111
III
III'
114 115
113
312
114 115
113
313
114 115
113

Fig. 47



333
320
(Vssl)281'
SST
(Vuwl)271"
MC6
(Vuwl)261'
MC5
2nd
Sub-Block
(Vuwl)251"
MC4
112'
(Vwe)241"
③
MC3
(Vwe)231'
②
MC2
1st
Sub-Block
(Vwe)221"
①
MC1
(Vgsl)211'
GST
311
(Vers)111
114
115
113

Fig. 48

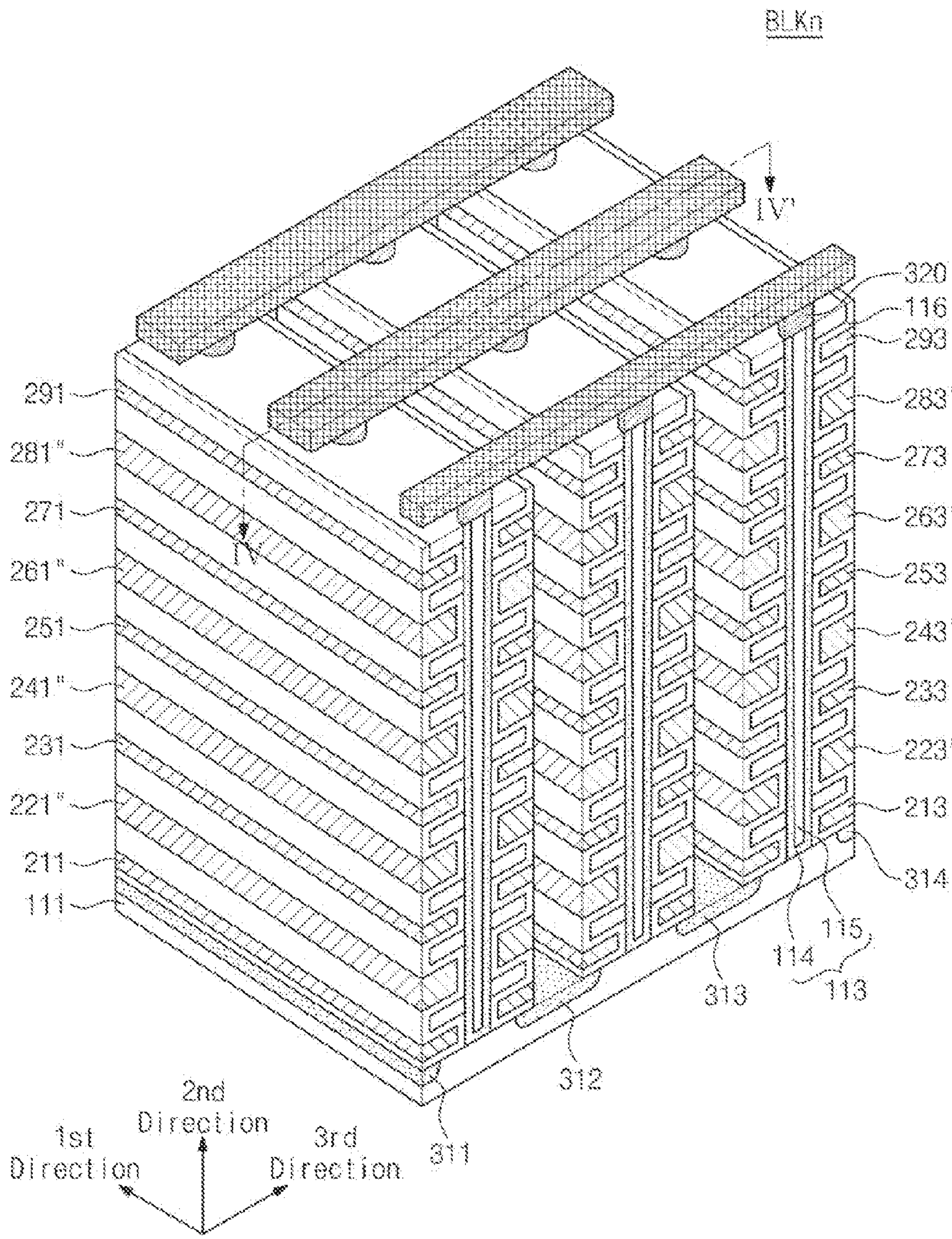

BLKn
IV'
IV
320
116
293
283"
273
263"
253
243"
233
223"
213
314
115
114
113
313
312
311
291
281"
271
261"
251
241"
231
221"
211
111
2nd Direction
1st Direction
3rd Direction

Fig. 49

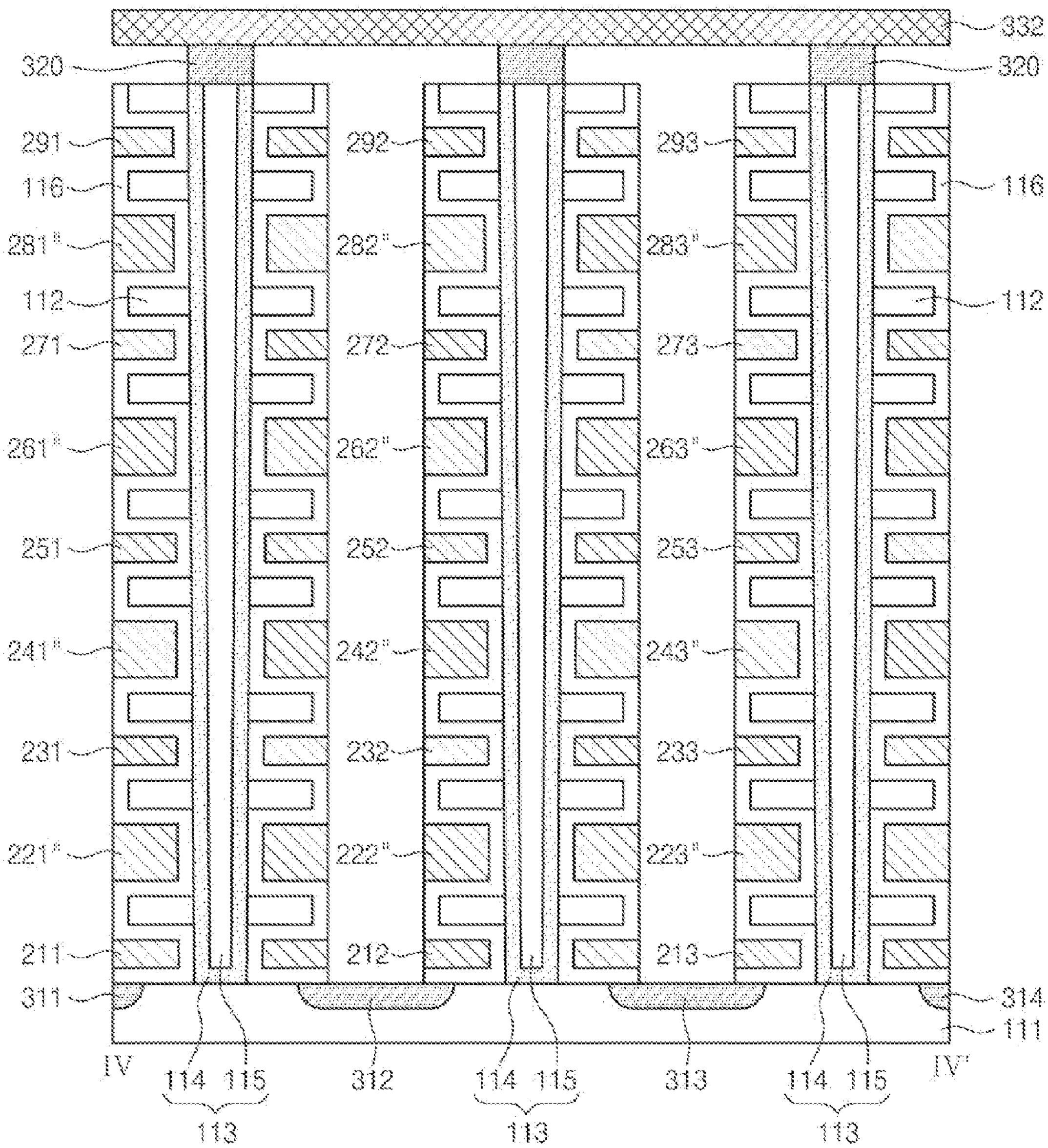

332
320
320
291
292
293
116
116
281"
282"
283"
112
112
271
272
273
261"
262"
263"
251
252
253
241"
242"
243"
231
232
233
221"
222"
223"
211
212
213
311
314
111
IV
IV'
114 115
312
114 115
313
114 115
113
113
113

Fig. 50

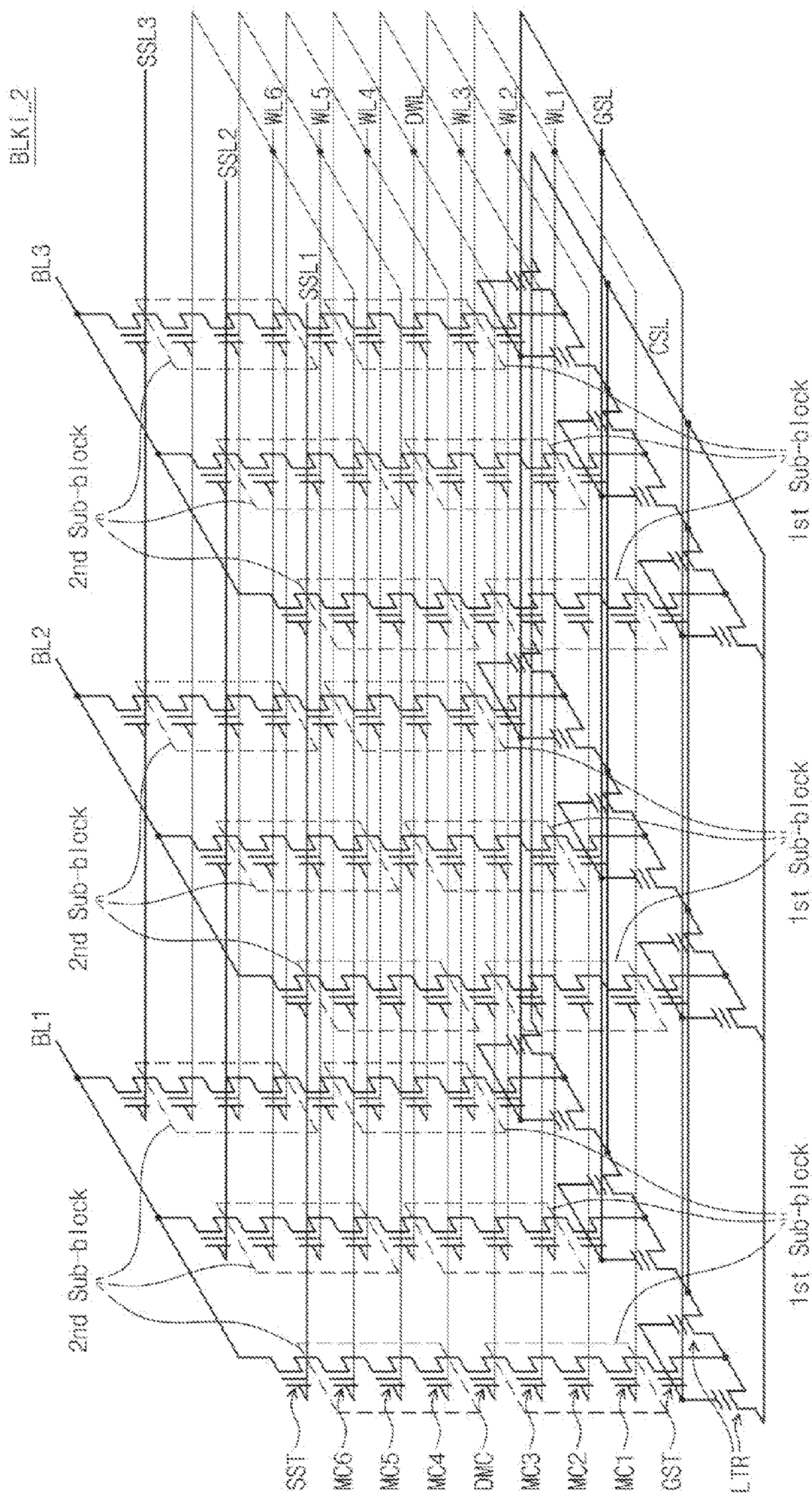

BLKi_2
SSL3
SSL2
SSL1
WL6
WL5
WL4
DWL
WL3
WL2
WL1
GSL
CSL
BL1
BL2
BL3
2nd Sub-block
2nd Sub-block
2nd Sub-block
1st Sub-block
1st Sub-block
1st Sub-block
SST
MC6
MC5
MC4
DMC
MC3
MC2
MC1
GST
LTR

Fig. 51

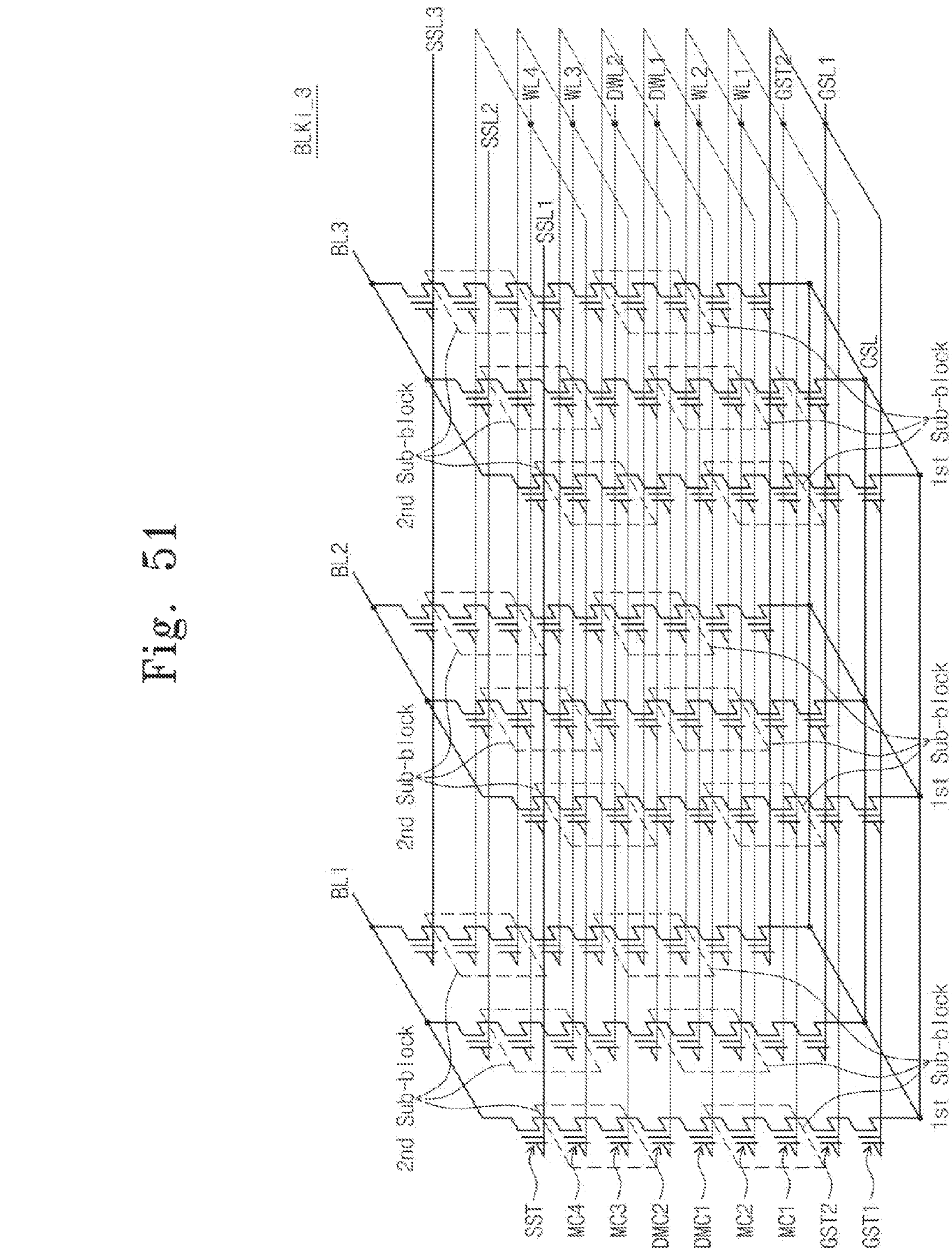

BLKi_3
SSL3
SSL2
SSL1
WL4
WL3
DWL2
DWL1
WL2
WL1
GST2
GSL1
BL1
BL2
BL3
2nd Sub-block
1st Sub-block
CSL
SST
MC4
MC3
DMC2
DMC1
MC2
MC1
GST2
GST1

Fig. 52

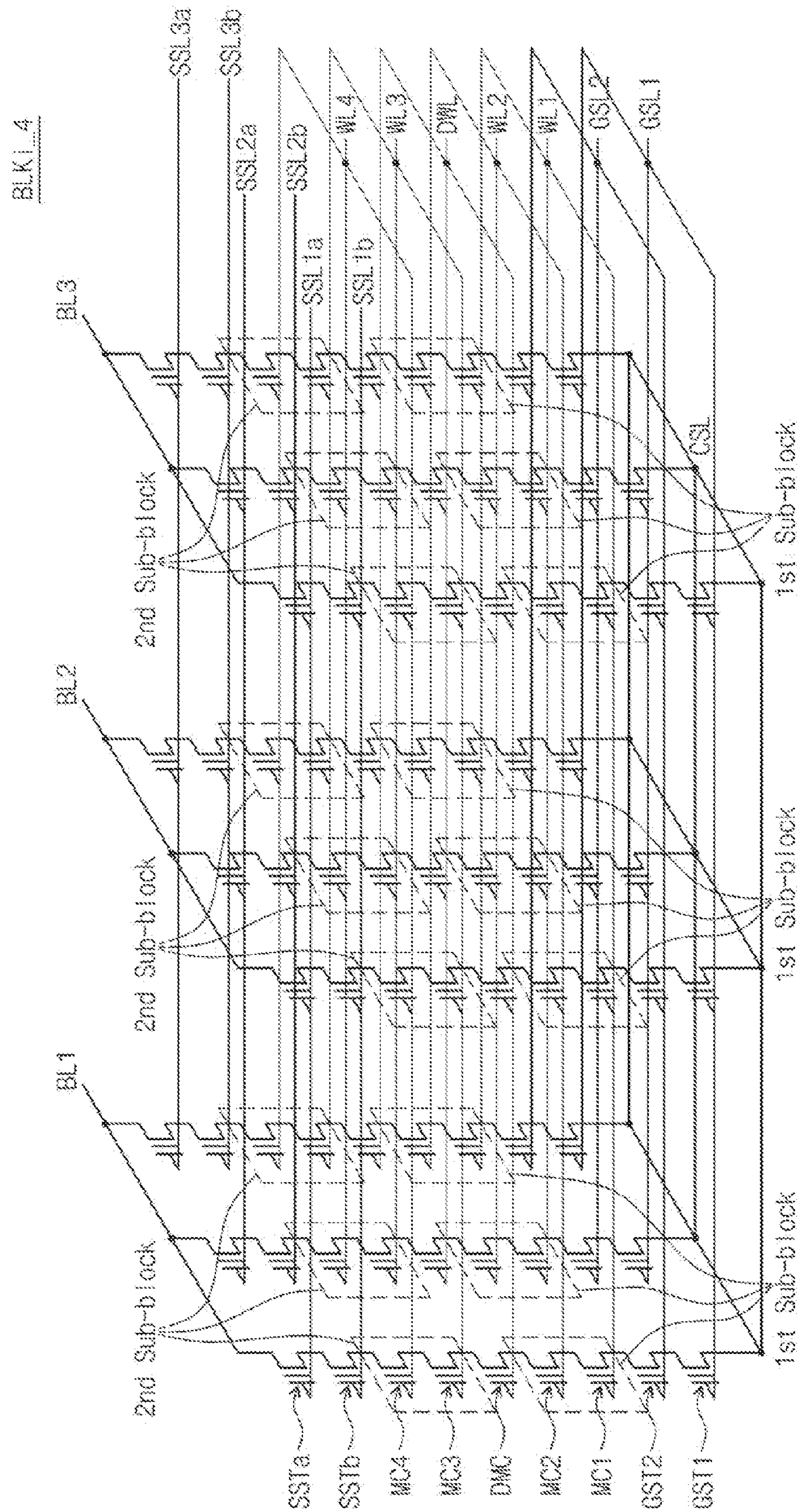

BLKi_4
SSL3a
SSL3b
SSL2a
SSL2b
WL4
WL3
DWL
WL2
WL1
GSL2
GSL1
BL3
SSL1a
SSL1b
CSL
BL2
BL1
2nd Sub-block
1st Sub-block
2nd Sub-block
1st Sub-block
2nd Sub-block
1st Sub-block
SSTa
SSTb
MC4
MC3
DMC
MC2
MC1
GST2
GST1

Fig. 53

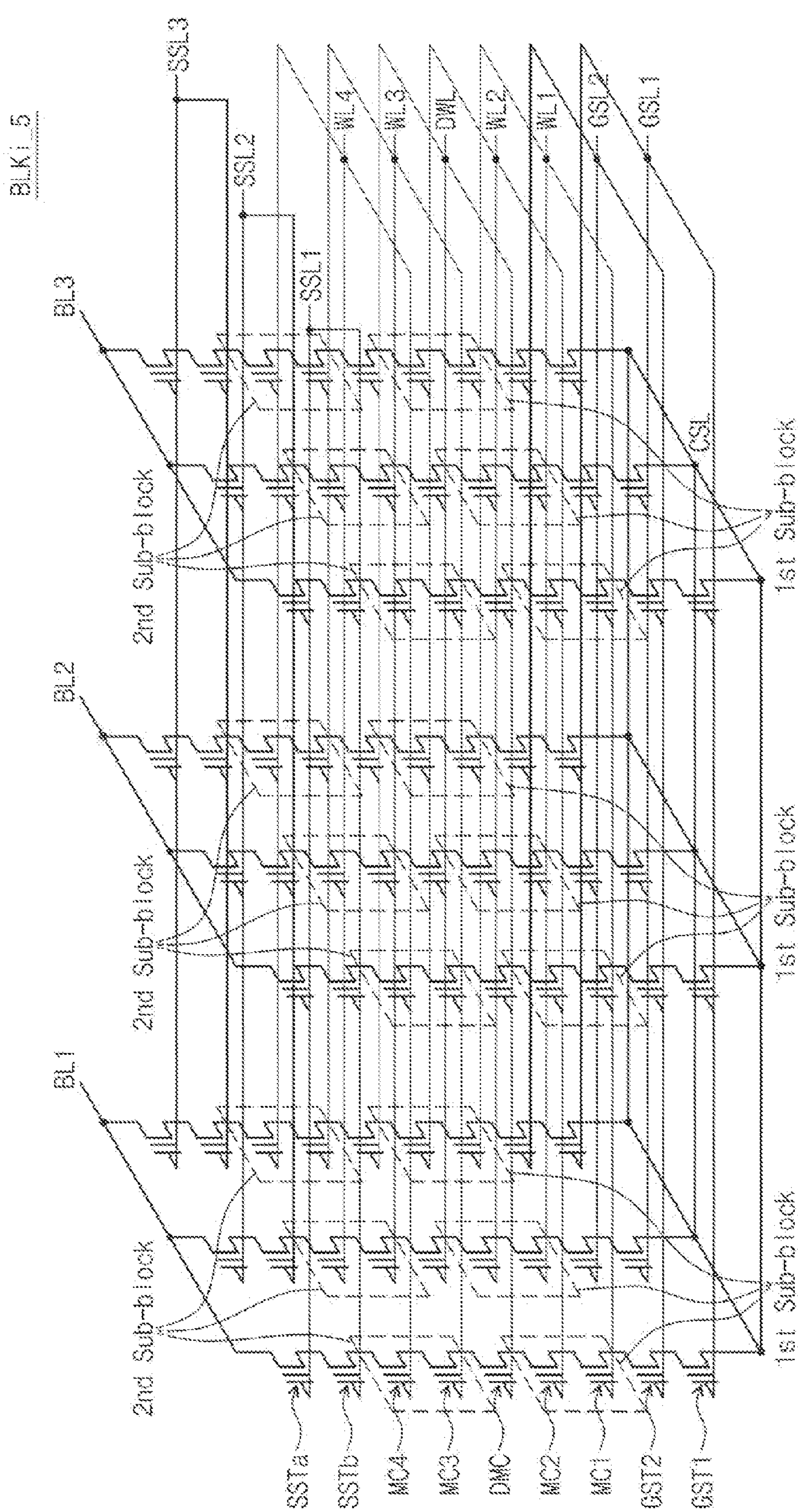
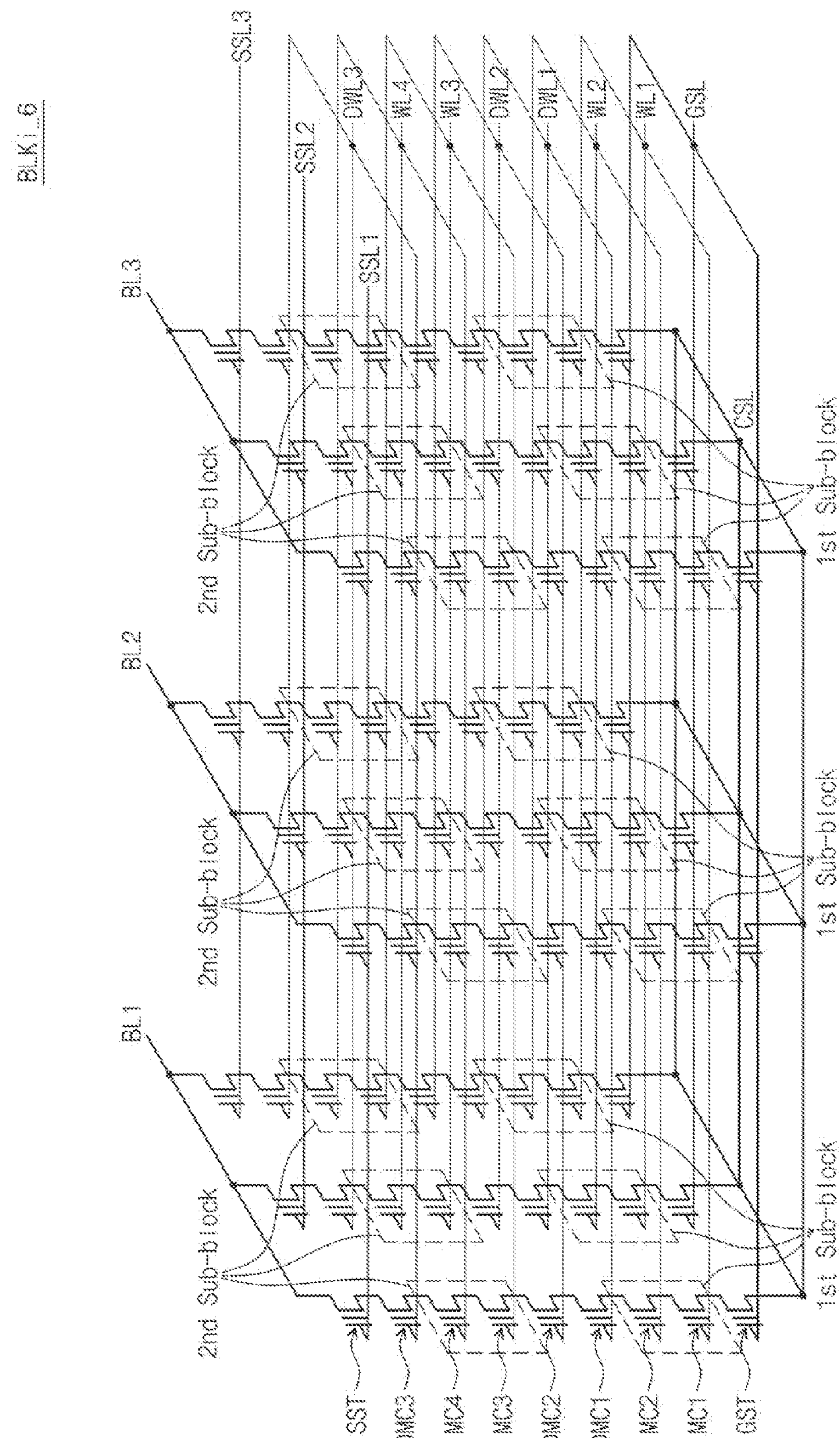

BLKi_5
SSL3
SSL2
SSL1
WL4
WL3
DWL
WL2
WL1
GSL2
GSL1
BL1
BL2
BL3
CSL
2nd Sub-block
1st Sub-block
SSTa
SSTb
MC4
MC3
DMC
MC2
MC1
GST2
GST1

Fig. 54



BLKi_6
SSL3
SSL2
SSL1
DWL3
WL4
WL3
DWL2
DWL1
WL2
WL1
GSL
BL1
BL2
BL3
CSL
2nd Sub-block
1st Sub-block
SST
DMC3
MC4
MC3
DMC2
DMC1
MC2
MC1
GST

Fig. 55

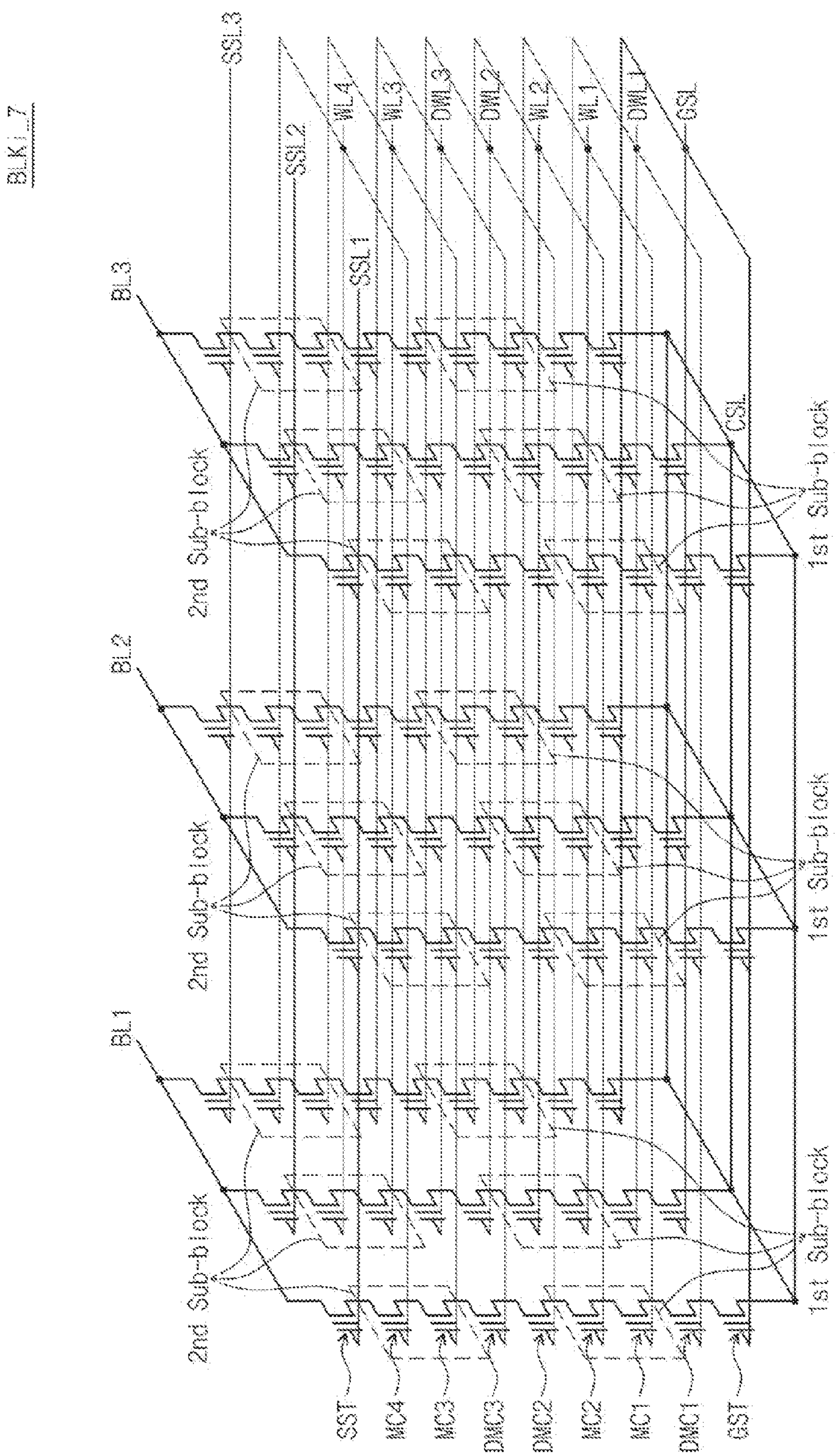

BLKi_7
BL1
BL2
BL3
SSL3
SSL2
SSL1
WL4
WL3
DWL3
DWL2
WL2
WL1
DWL1
GSL
CSL
2nd Sub-block
1st Sub-block
SST
MC4
MC3
DMC3
DMC2
MC2
MC1
DMC1
GST

Fig. 56

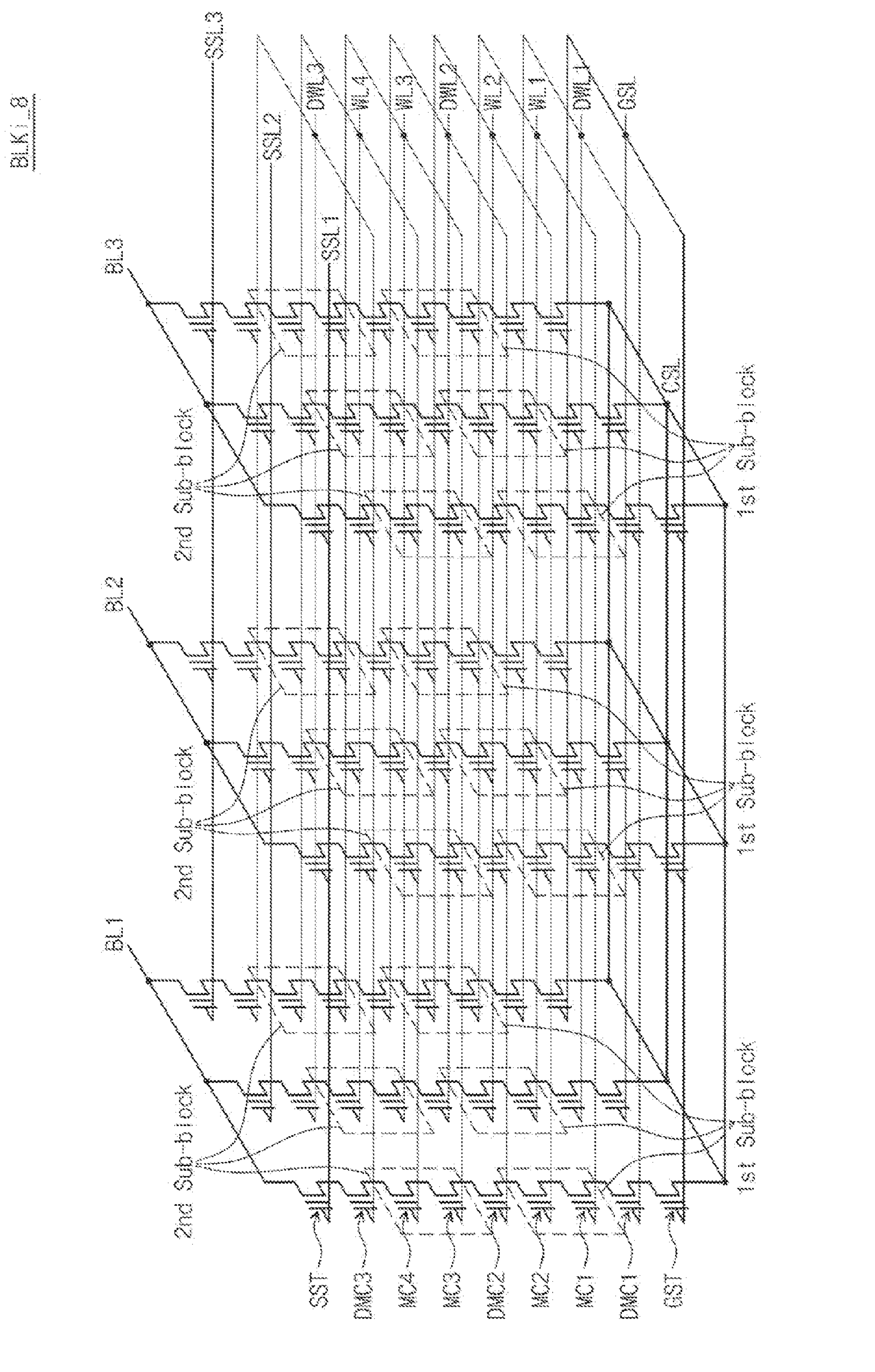

BLKi_8
BL1
BL2
BL3
SSL1
SSL2
SSL3
DWL3
WL4
WL3
DWL2
WL2
WL1
DWL1
GSL
2nd Sub-block
1st Sub-block
SST
DMC3
MC4
MC3
DMC2
MC2
MC1
DMC1
GST

Fig. 57

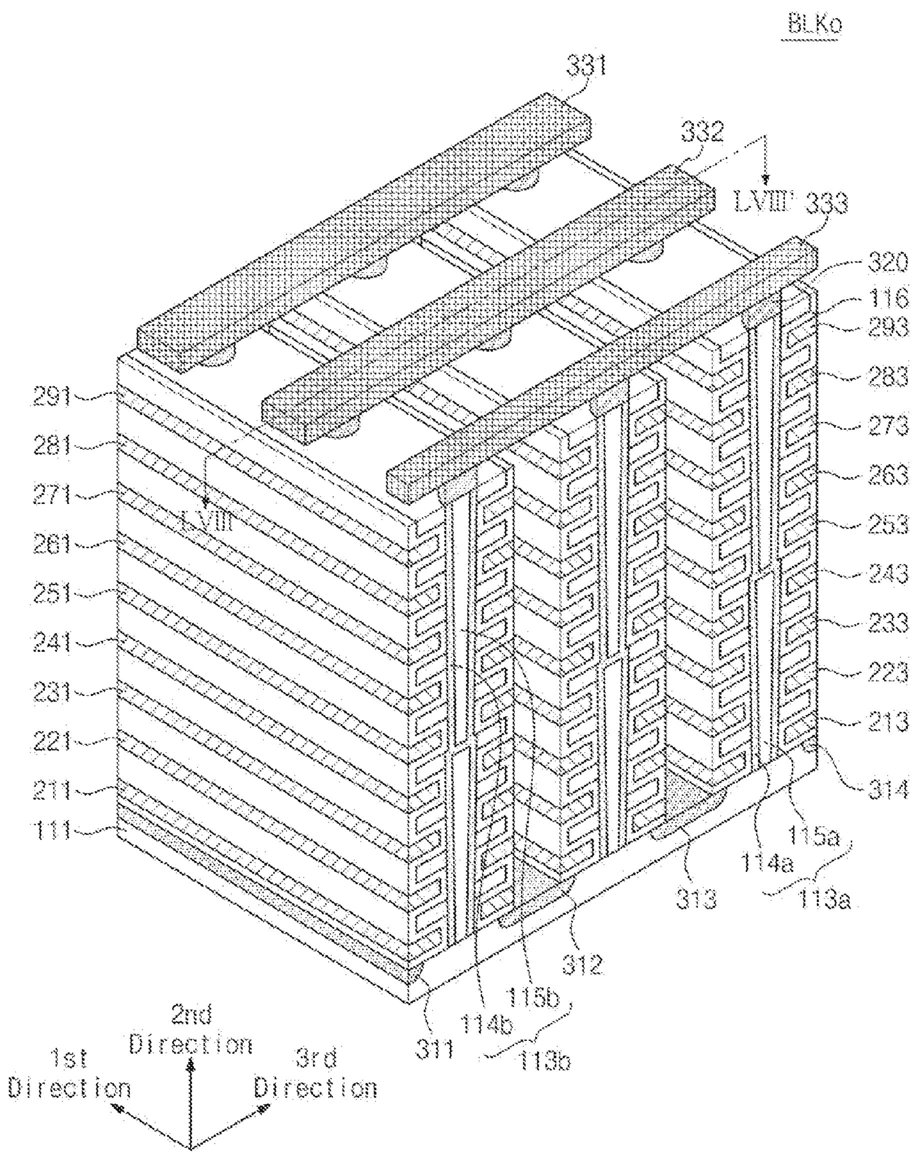

BLKo
331
332
LVIII'
333
320
116
293
283
273
263
253
243
233
223
213
314
115a
114a
113a
313
312
291
281
271
261
251
241
231
221
211
111
LVIII
115b
114b
113b
311
2nd Direction
1st Direction
3rd Direction

Fig. 58

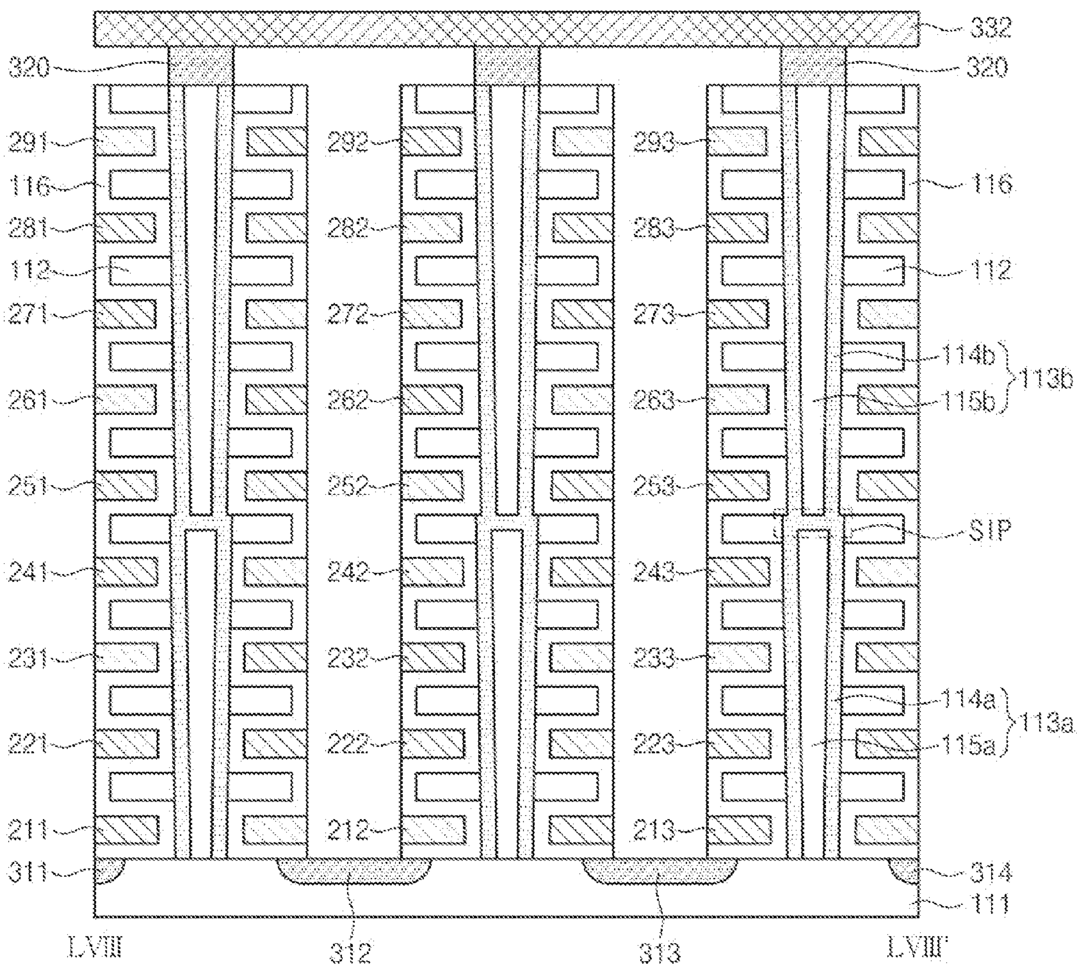
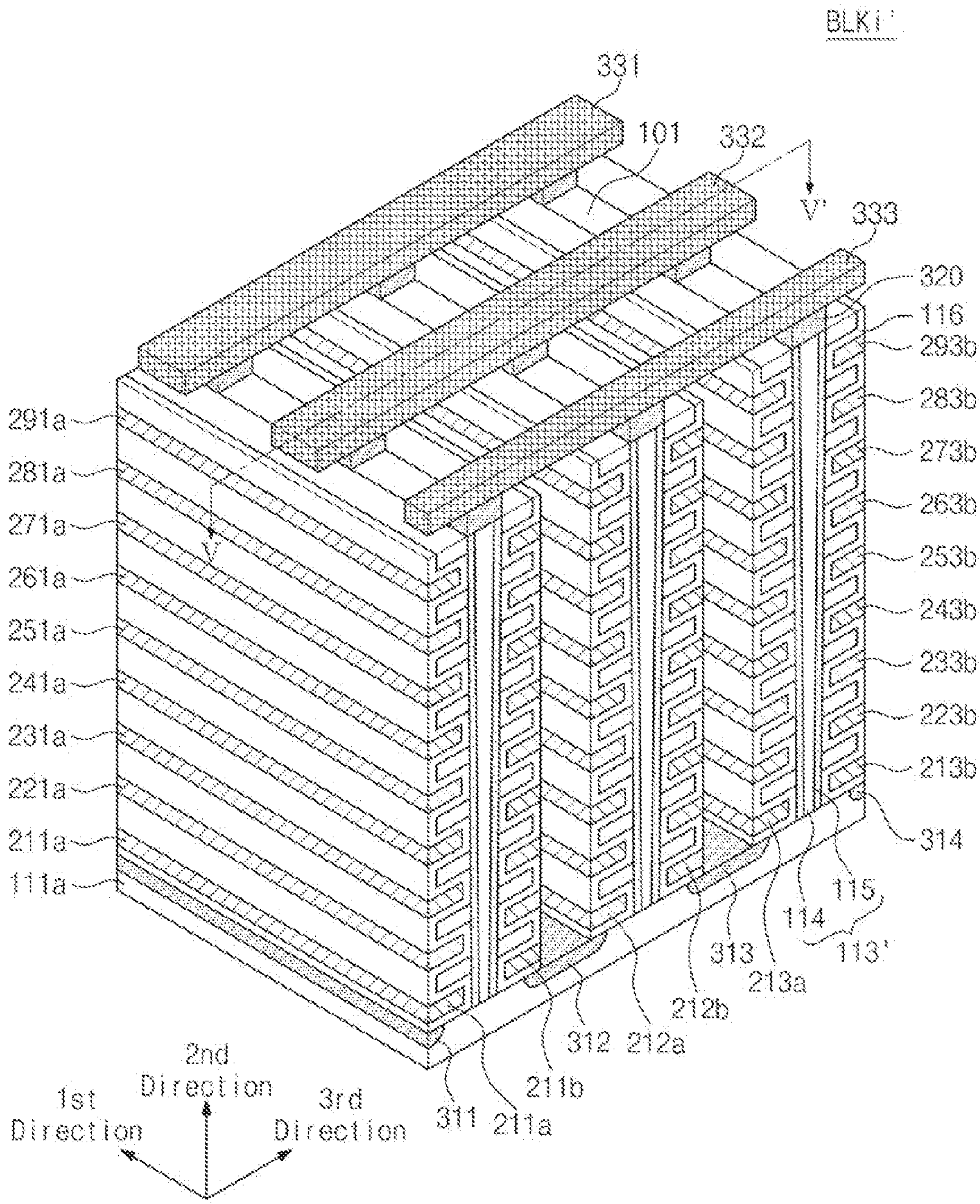

332
320
320
291
292
293
116
116
281
282
283
112
112
271
272
273
114b
113b
261
262
263
115b
251
252
253
SIP
241
242
243
231
232
233
114a
113a
221
222
223
115a
211
212
213
311
314
111
LVIII
312
313
LVIII'

Fig. 59



BLKi'
331
101
332
V'
333
320
116
293b
283b
273b
263b
253b
243b
233b
223b
213b
314
291a
281a
271a
V
261a
251a
241a
231a
221a
211a
111a
115
114
113'
313
213a
212b
312
212a
211b
311
211a
2nd Direction
1st Direction
3rd Direction

Fig. 60

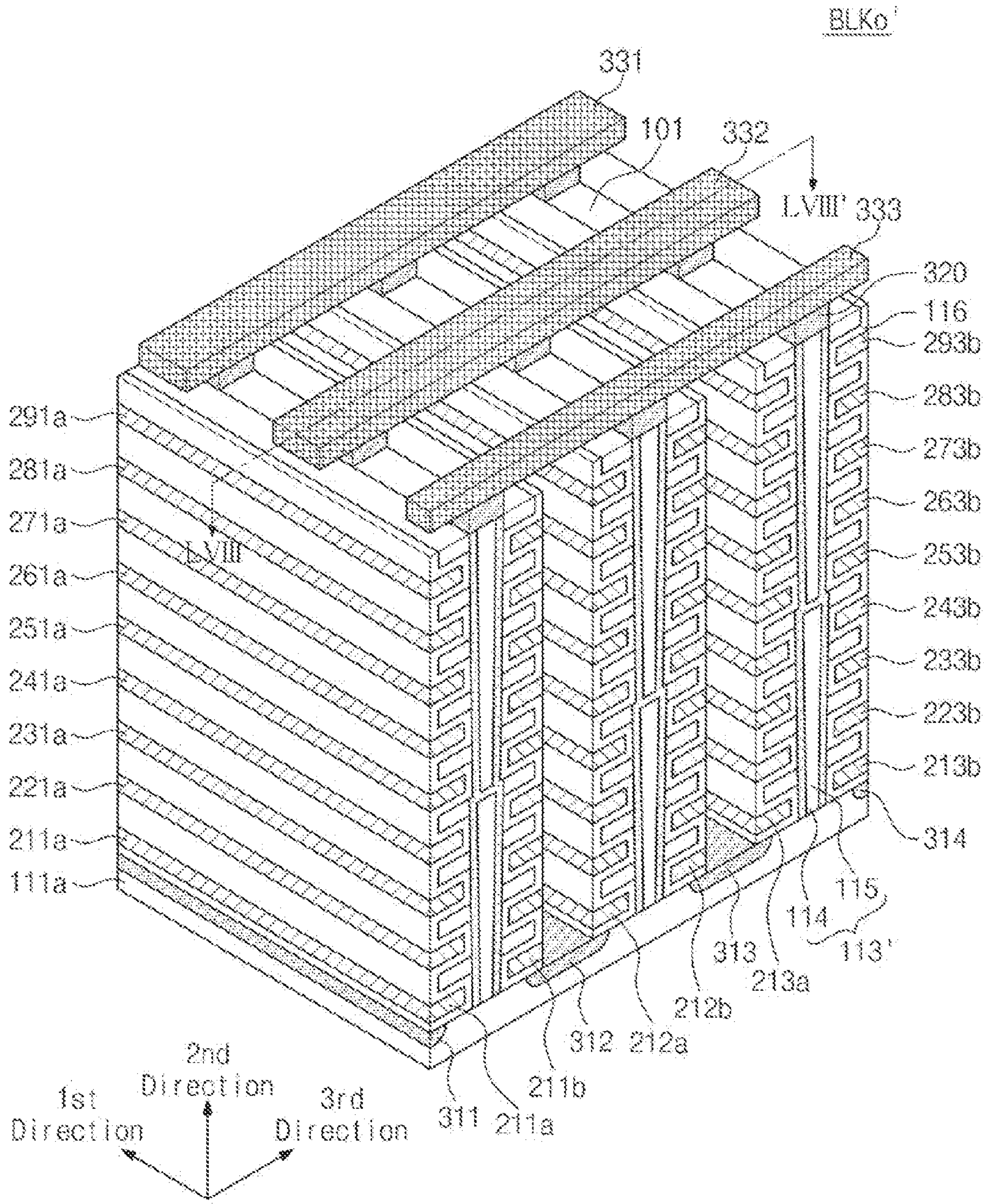

BLKo'
331
101
332
LVIII'
333
320
116
293b
283b
273b
263b
253b
243b
233b
223b
213b
314
291a
281a
271a
LVIII
261a
251a
241a
231a
221a
211a
111a
115
114
113'
313
213a
212b
312
212a
211b
311
211a
2nd Direction
1st Direction
3rd Direction

Fig. 61

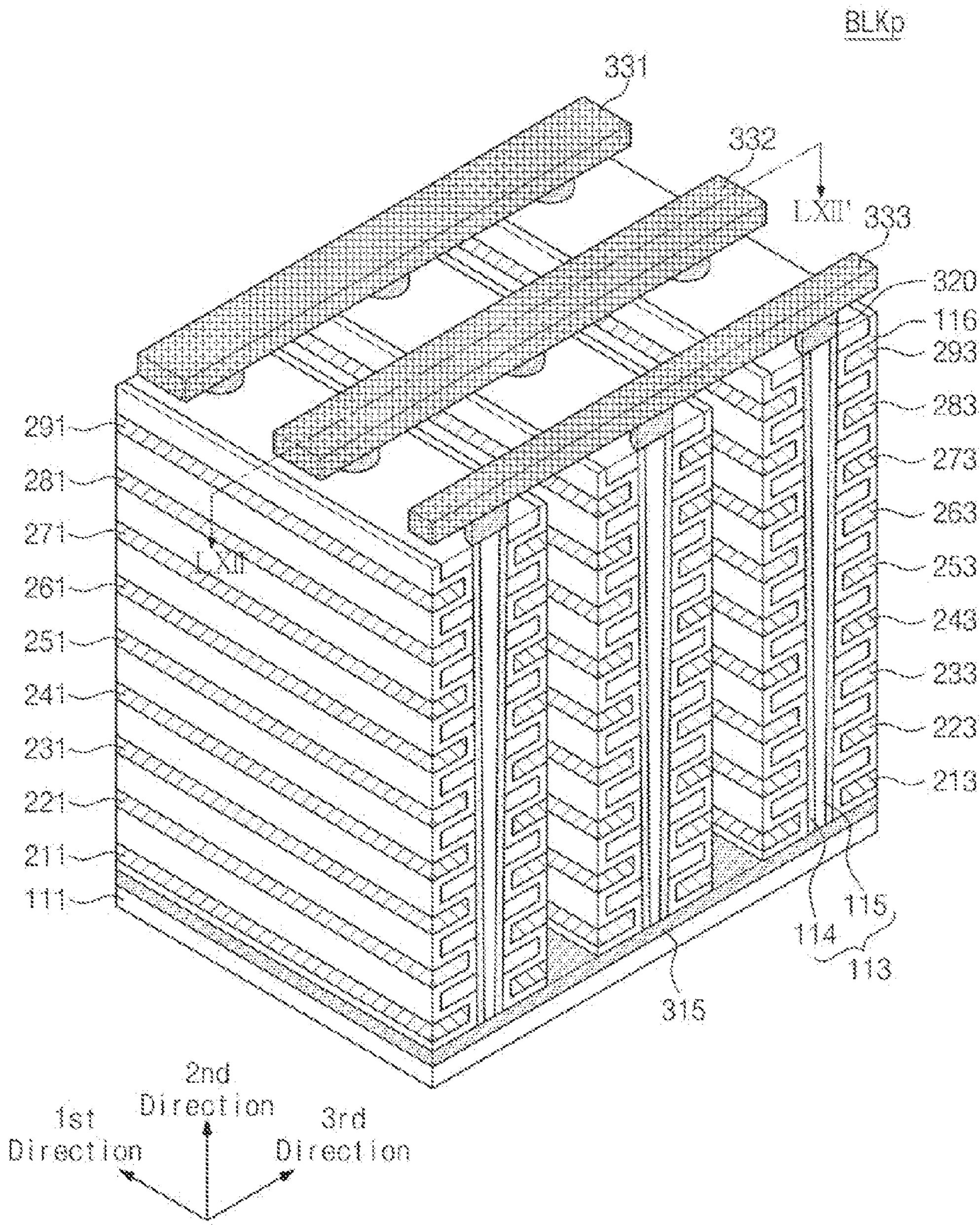

BLKp
331
332
LXII'
333
320
116
293
283
273
263
253
243
233
223
213
291
281
271
LXII
261
251
241
231
221
211
111
114
115
113
315
2nd
Direction
1st
Direction
3rd
Direction

Fig. 62

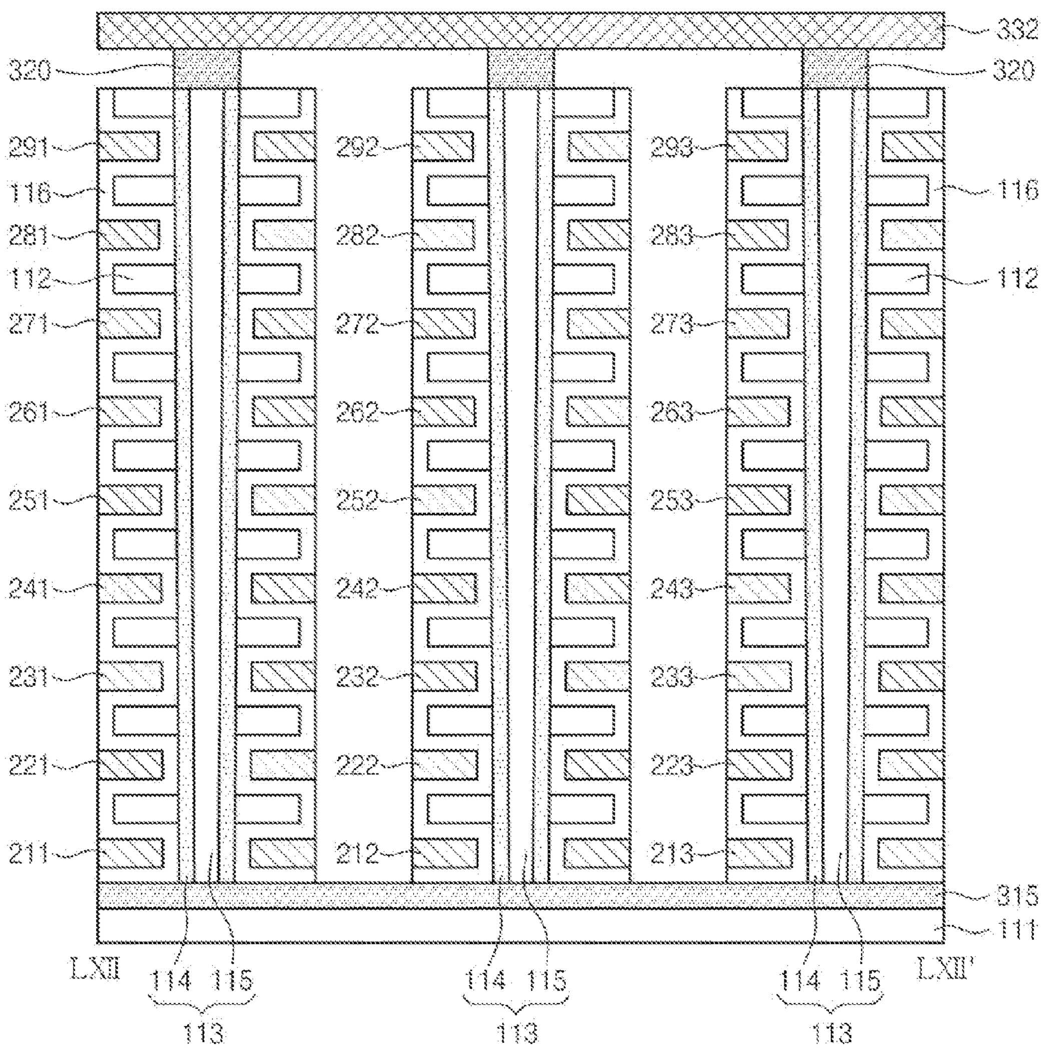

332
320
320
291
116
281
112
271
261
251
241
231
221
211
292
282
272
262
252
242
232
222
212
293
283
273
263
253
243
233
223
213
116
112
315
111
LXII
LXII'
114
115
113

Fig. 63

SSL	Float
WLs of unselected sub block	Float
WLs of selected sub block	Float → Vwe2
DWL	Vdwl3
GSL	Vss → Float
Substrate	Vpre → Vers2

Fig. 64

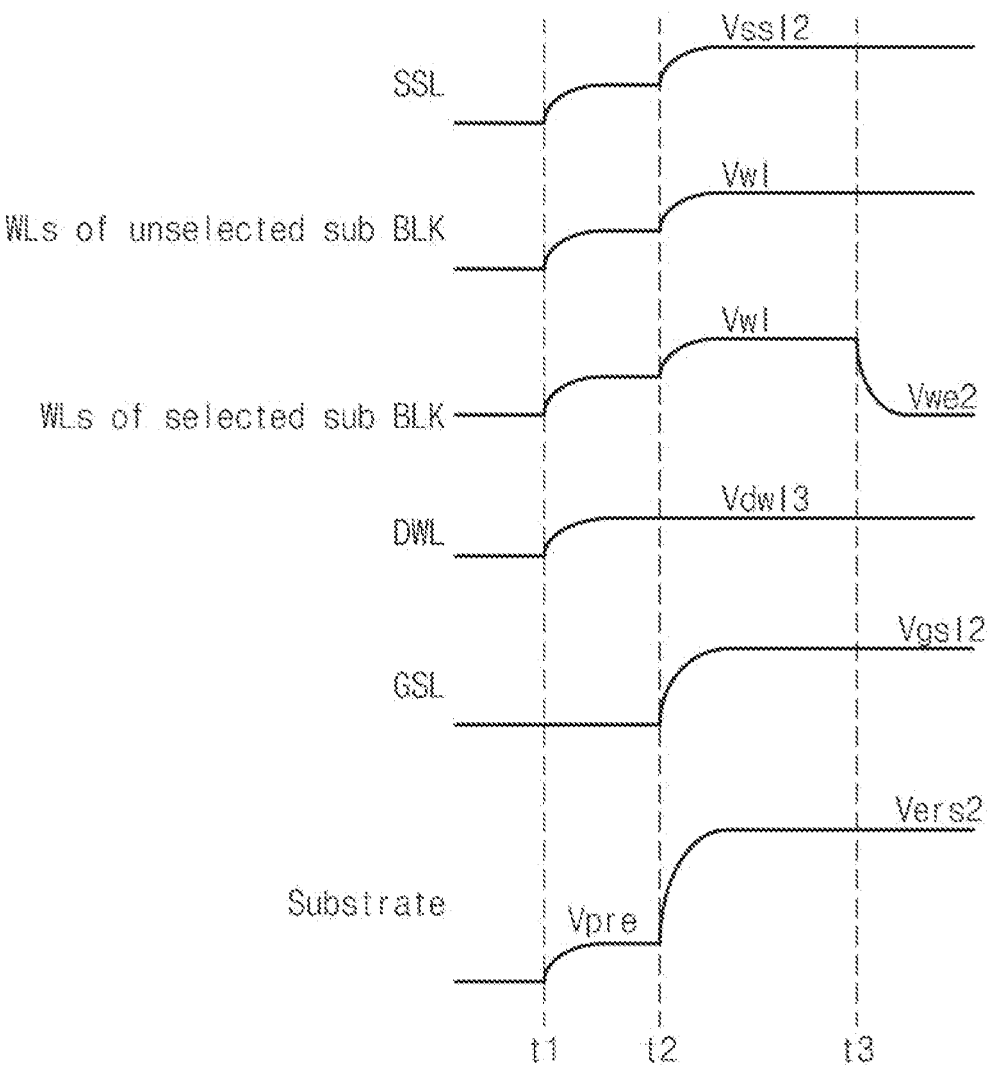
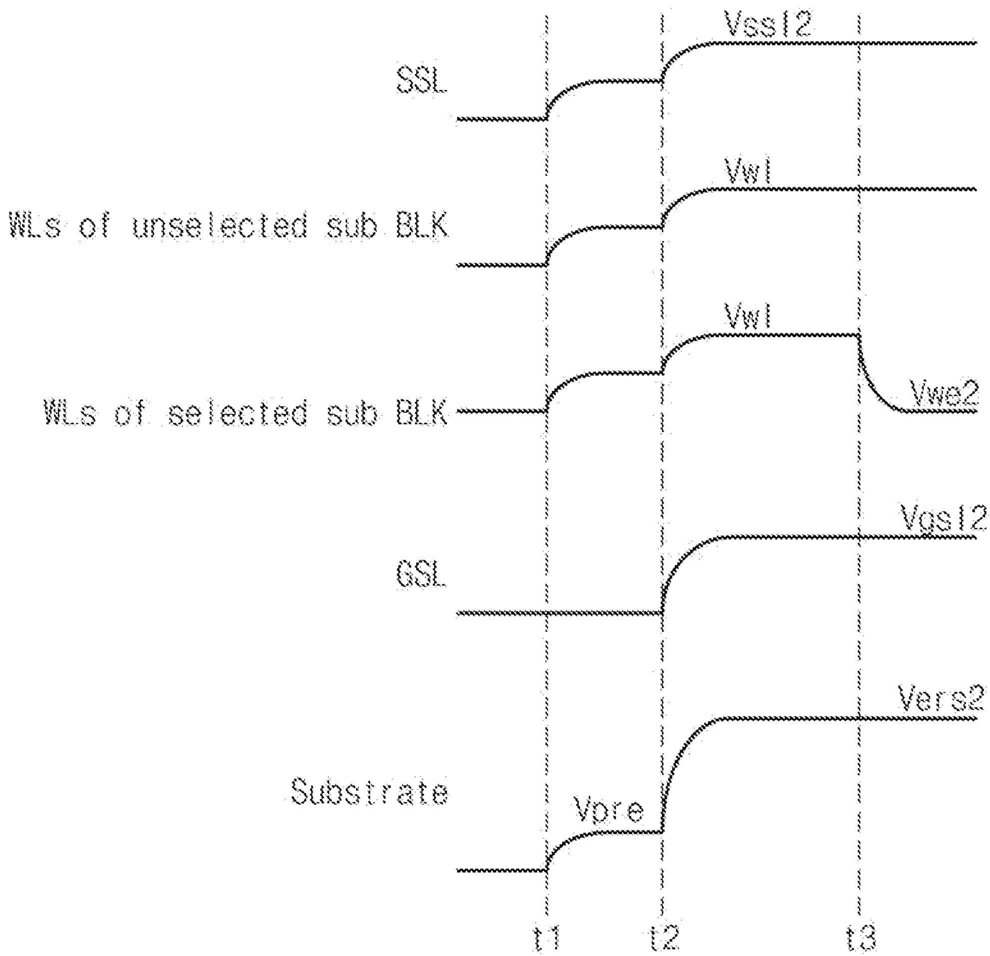

SSL
Vssl2
WLs of unselected sub BLK
Vwl
WLs of selected sub BLK
Vwl
Vwe2
DWL
Vdwl3
GSL
Vgsl2
Substrate
Vpre
Vers2
t1
t2
t3

Fig. 65

SSL	Float
WLs of unselected sub block	Float
WLs of selected sub block	Float → Vwe2
GSL	Vss → Float
Substrate	Vpre → Vers2

Fig. 66



SSL
Vssl2
WLs of unselected sub BLK
Vwl
WLs of selected sub BLK
Vwl
Vwe2
GSL
Vgsl2
Substrate
Vpre
Vers2
t1
t2
t3

Fig. 67

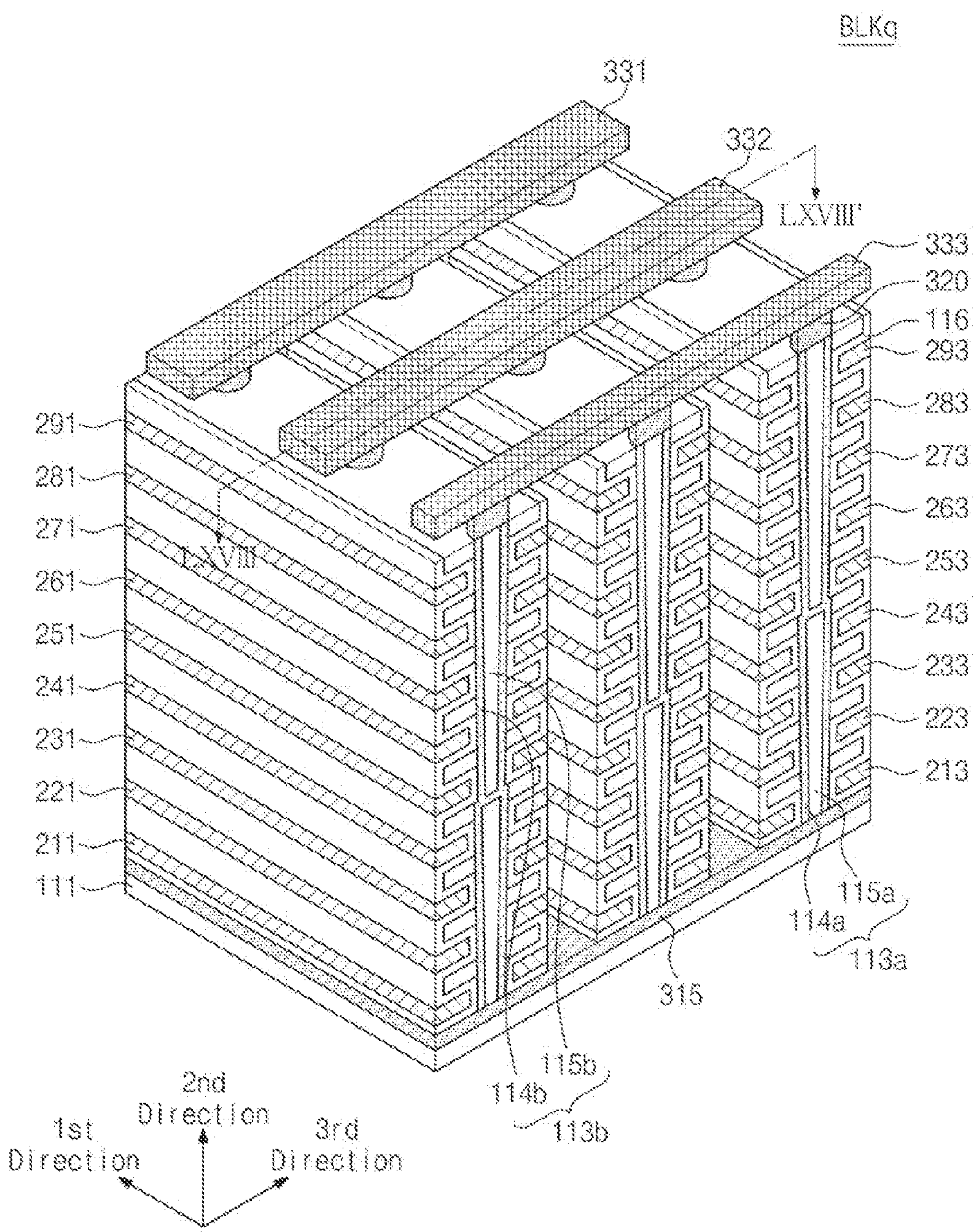

BLKq
331
332
LXVIII'
333
320
116
293
283
273
263
253
243
233
223
213
291
281
271
261
251
241
231
221
211
111
LXVIII
115a
114a
113a
315
115b
114b
113b
2nd
Direction
1st
Direction
3rd
Direction

Fig. 68

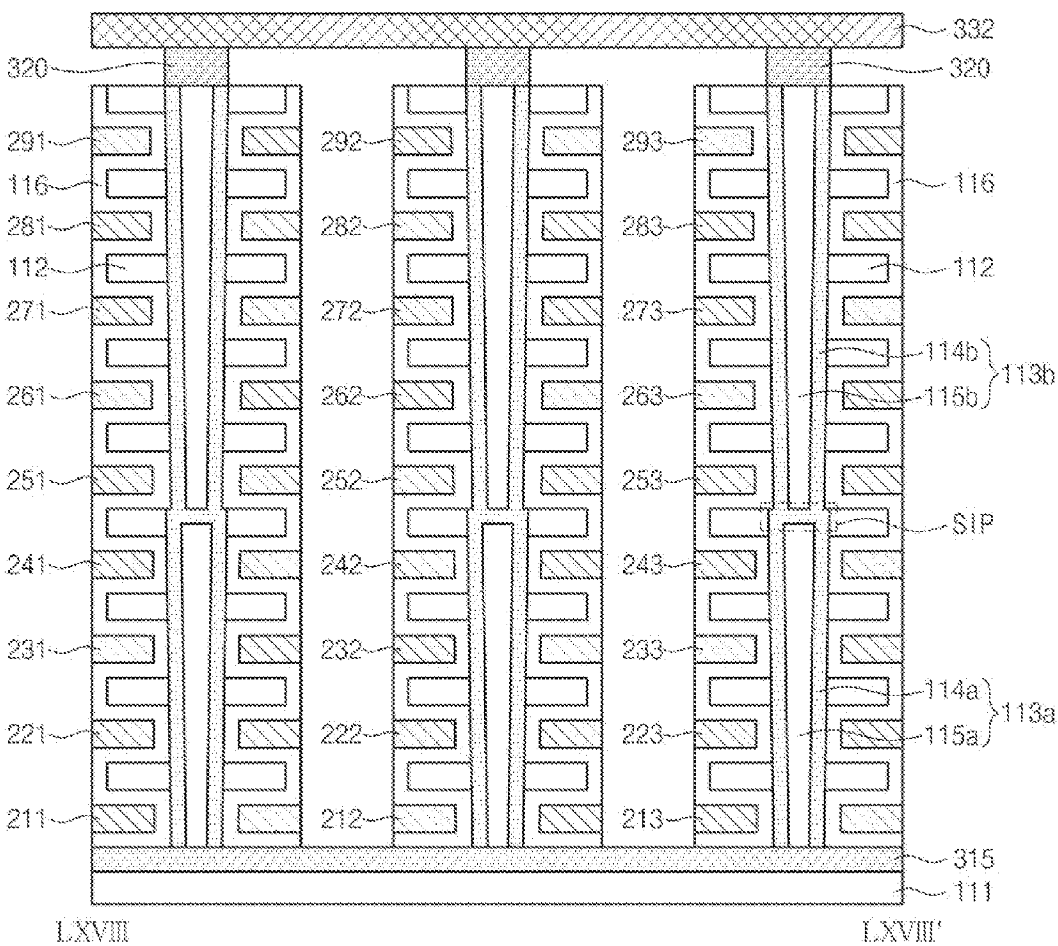

332
320
320
291
292
293
116
116
281
282
283
112
112
271
272
273
114b
113b
261
262
263
115b
251
252
253
SIP
241
242
243
231
232
233
114a
113a
221
222
223
115a
211
212
213
315
111
LXVIII
LXVIII'

Fig. 69

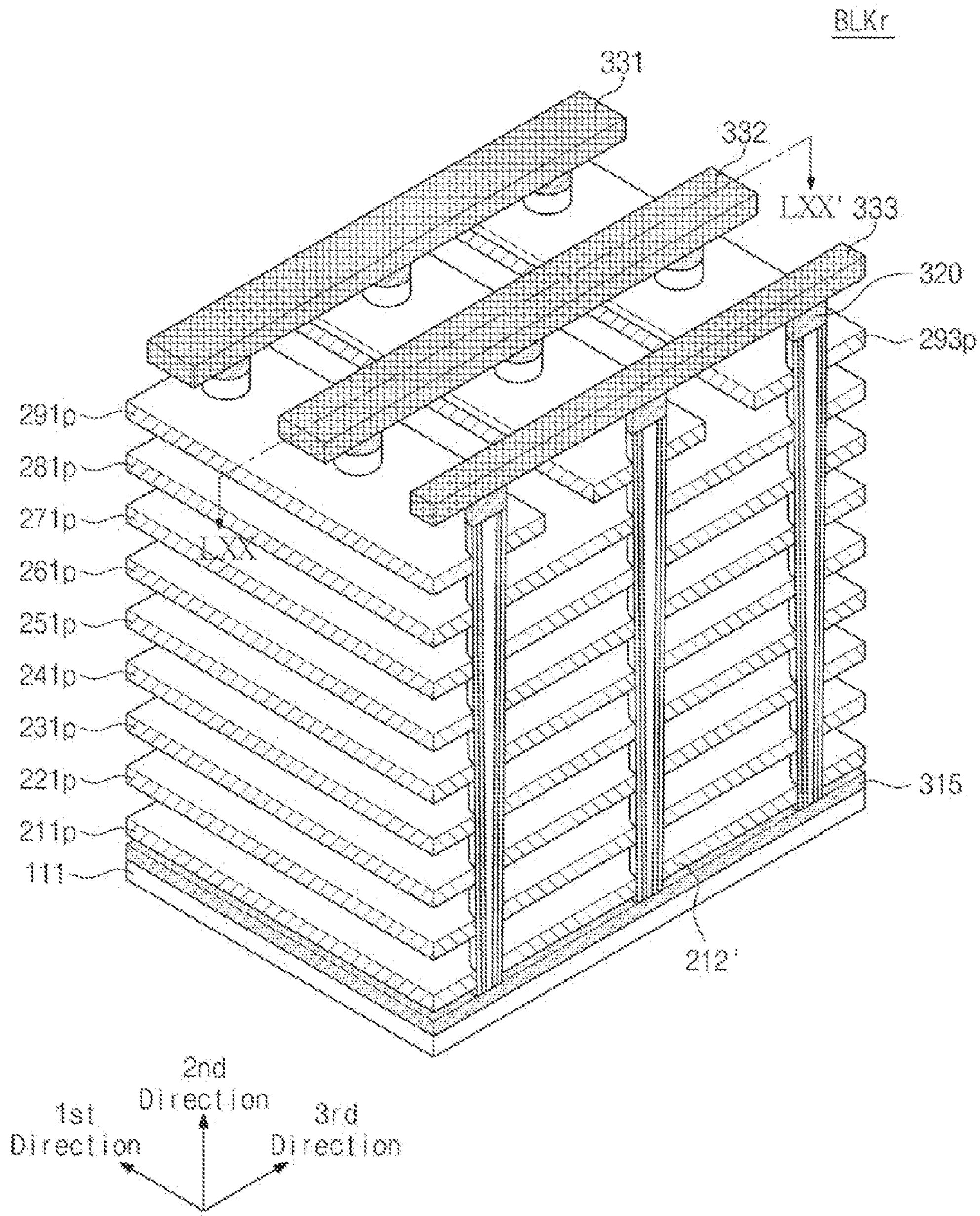

BLKr
331
332
LXX'
333
320
293p
291p
281p
271p
LXX
261p
251p
241p
231p
221p
211p
111
315
212'
2nd
Direction
1st
Direction
3rd
Direction

Fig. 70

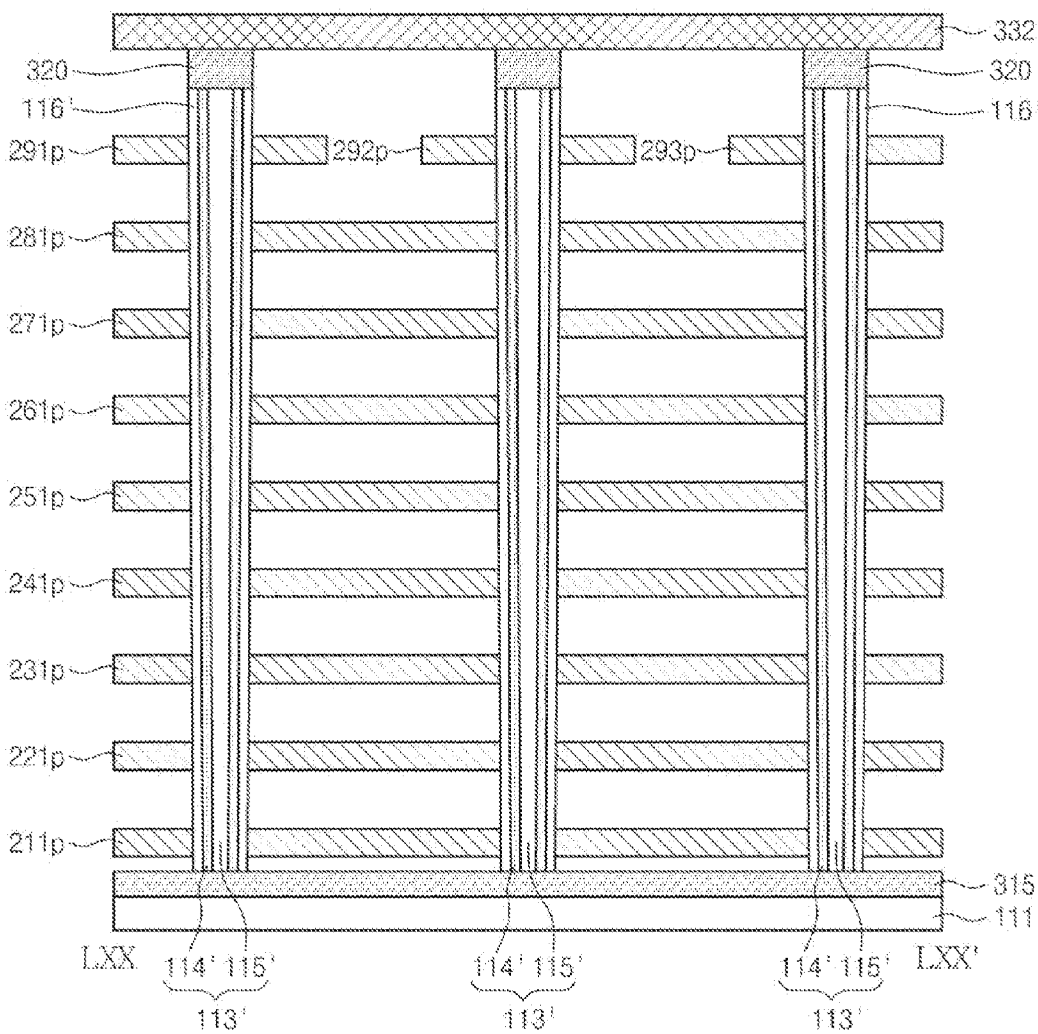

332
320
320
116'
116'
291p
292p
293p
281p
271p
261p
251p
241p
231p
221p
211p
315
111
LXX
LXX'
114' 115'
114' 115'
114' 115'
113'
113'
113'

Fig. 71

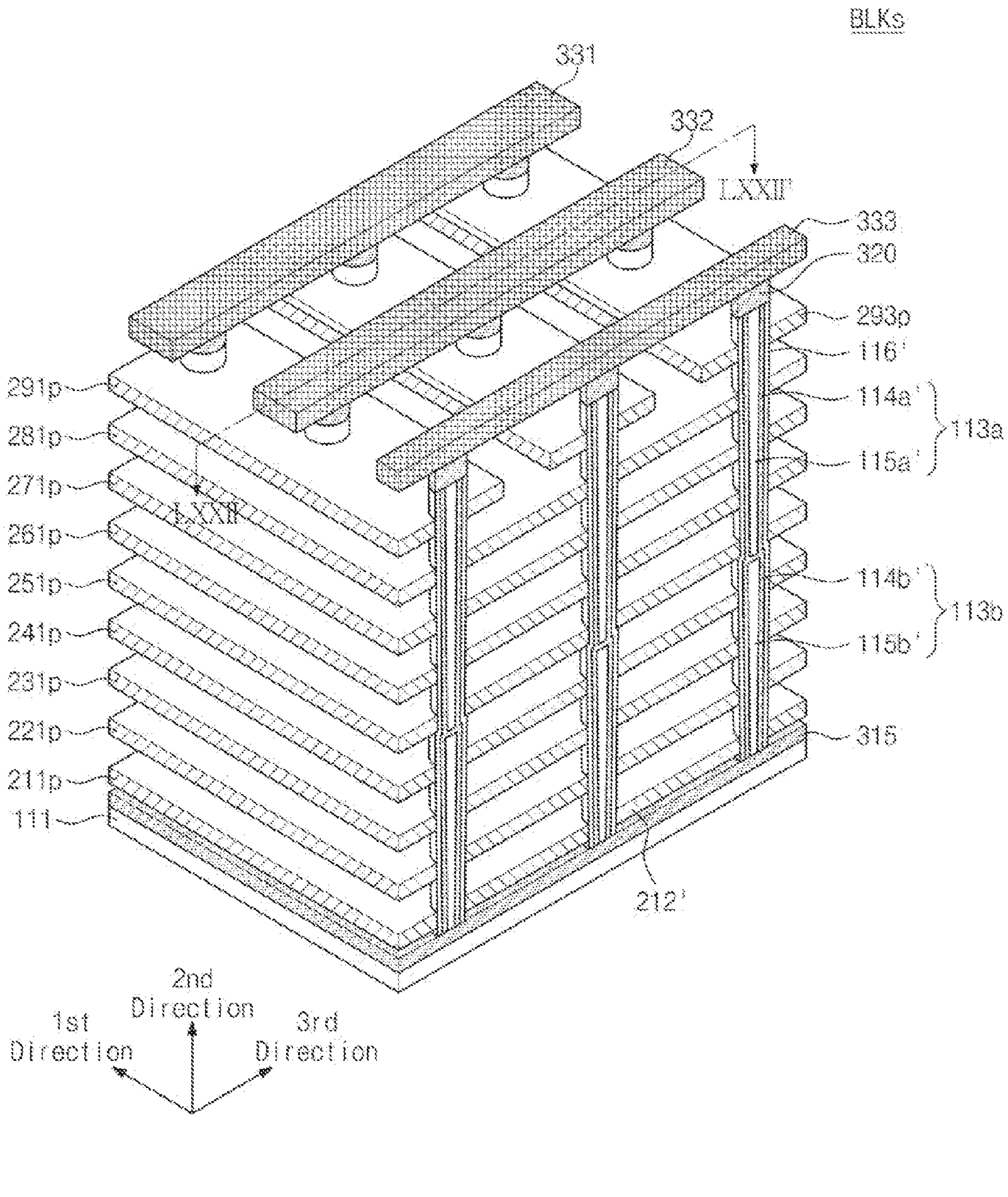

BLKs
331
332
LXXII'
333
320
293p
116'
114a'
113a'
115a'
114b'
113b'
115b'
315
291p
281p
271p
LXXII
261p
251p
241p
231p
221p
211p
111
212'
2nd Direction
1st Direction
3rd Direction

Fig. 72

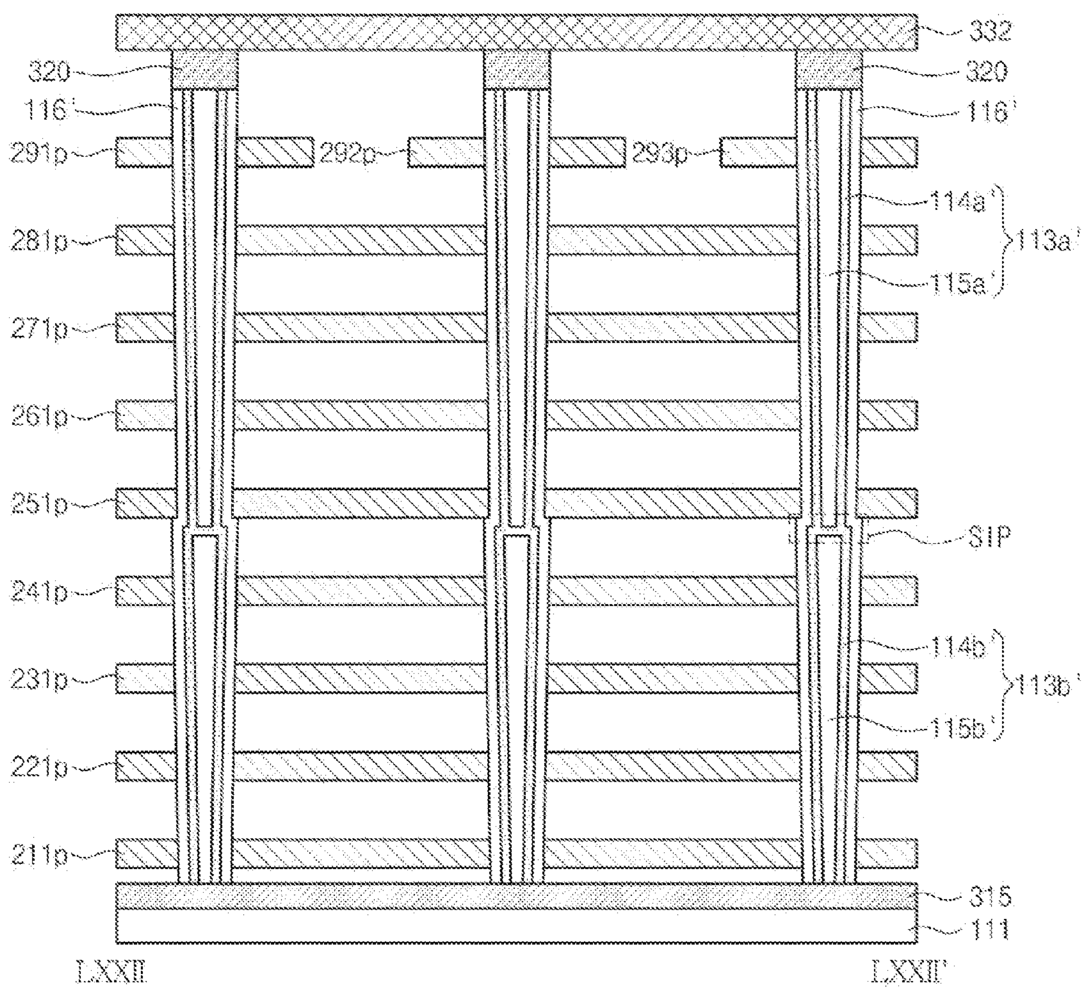

332
320
320
116'
116'
291p
292p
293p
114a'
113a'
115a'
281p
271p
261p
251p
SIP
241p
114b'
113b'
115b'
231p
221p
211p
315
111
LXXII
LXXII'

Fig. 73

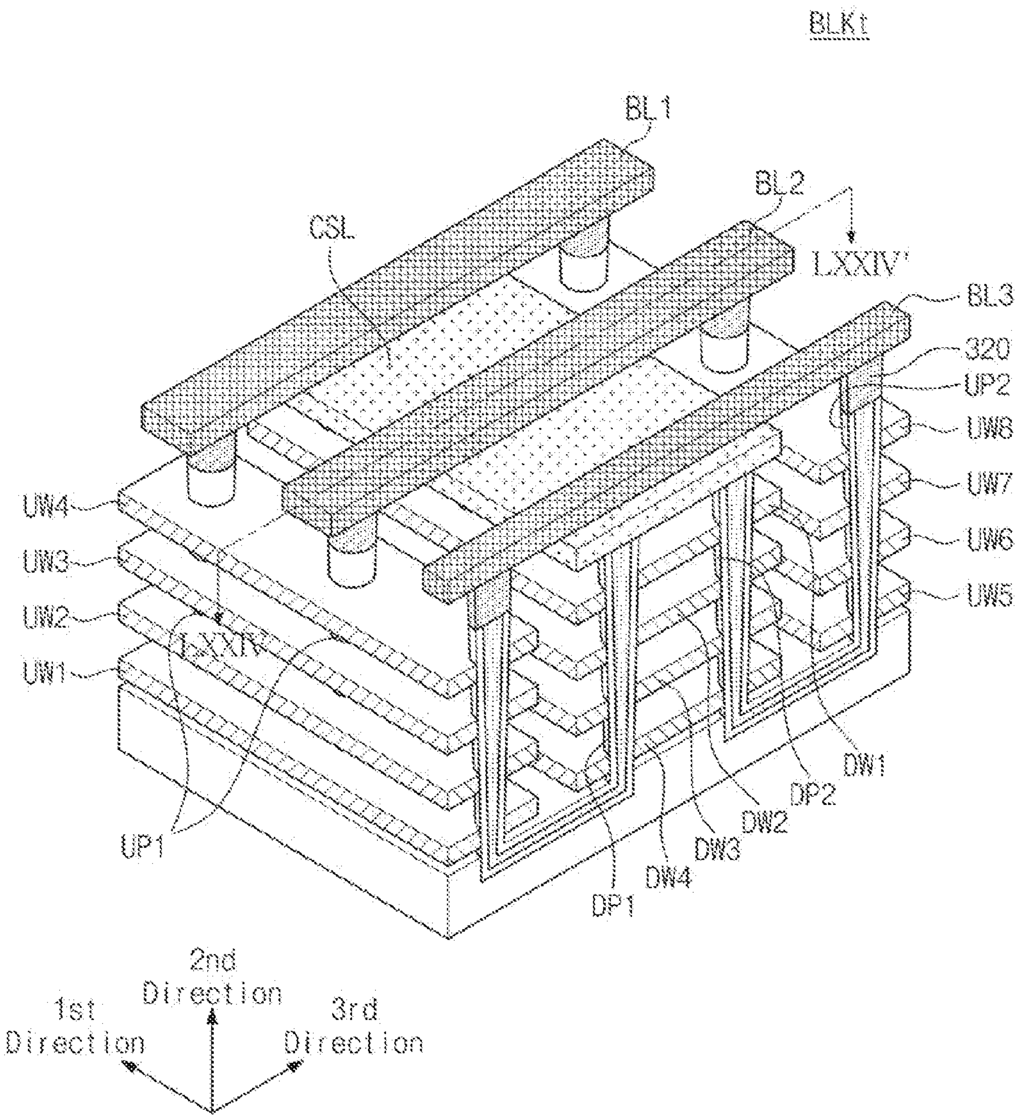

BLKt
BL1
BL2
BL3
CSL
LXXIV'
LXXIV
320
UP2
UW8
UW7
UW6
UW5
UW4
UW3
UW2
UW1
UP1
DP1
DW4
DW3
DW2
DP2
DW1
2nd Direction
1st Direction
3rd Direction

Fig. 74

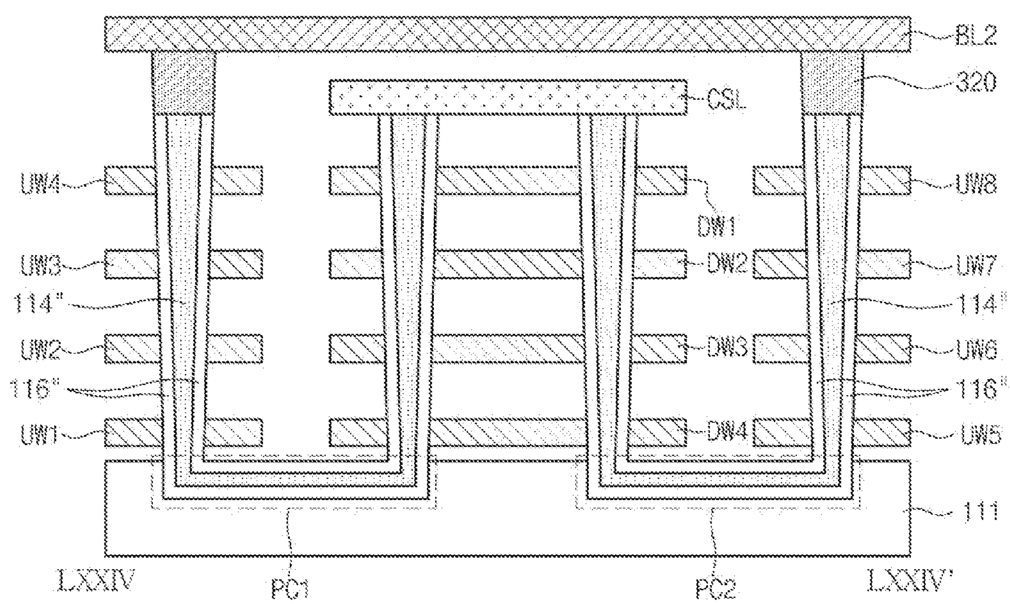

BL2
320
CSL
UW4
UW8
DW1
UW3
DW2
UW7
114"
114"
UW2
DW3
UW6
116"
116"
UW1
DW4
UW5
111
LXXIV
PC1
PC2
LXXIV'

Fig. 75

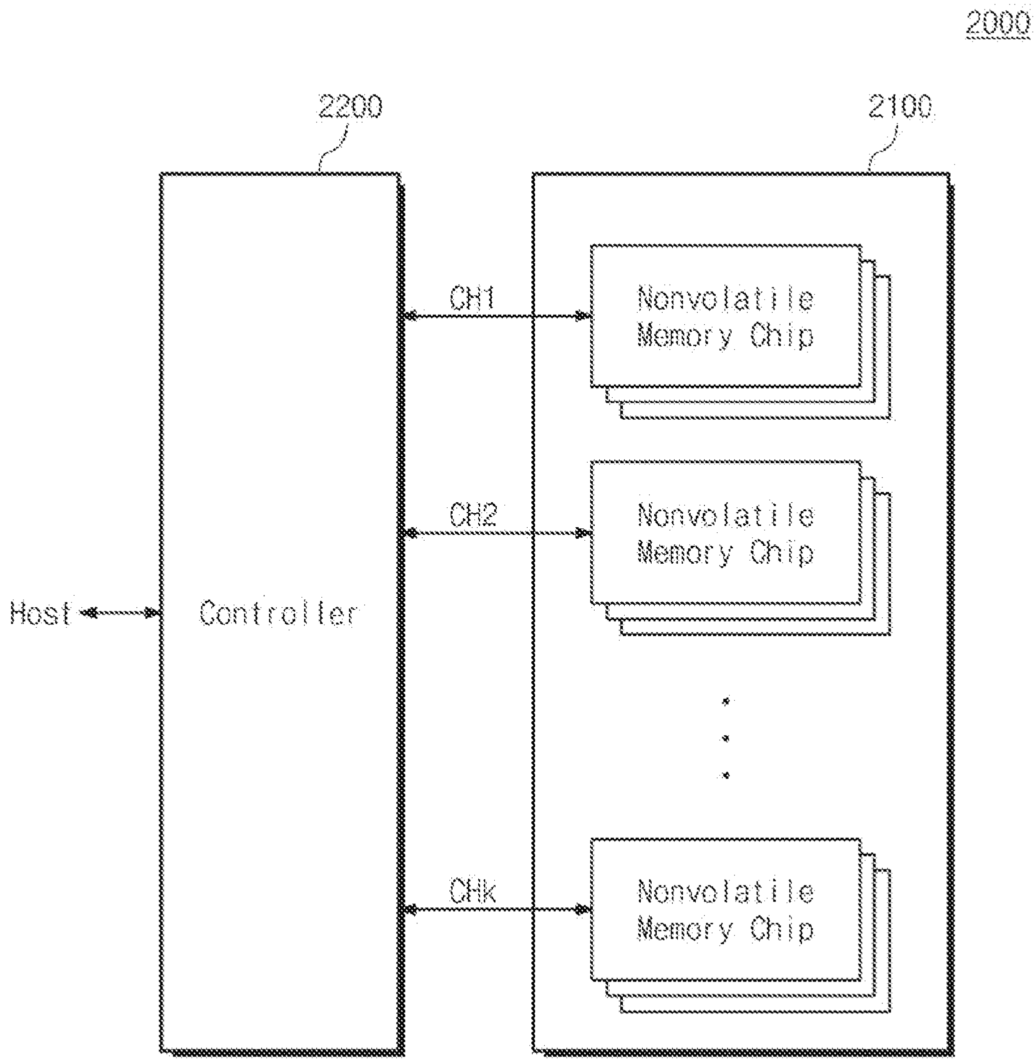
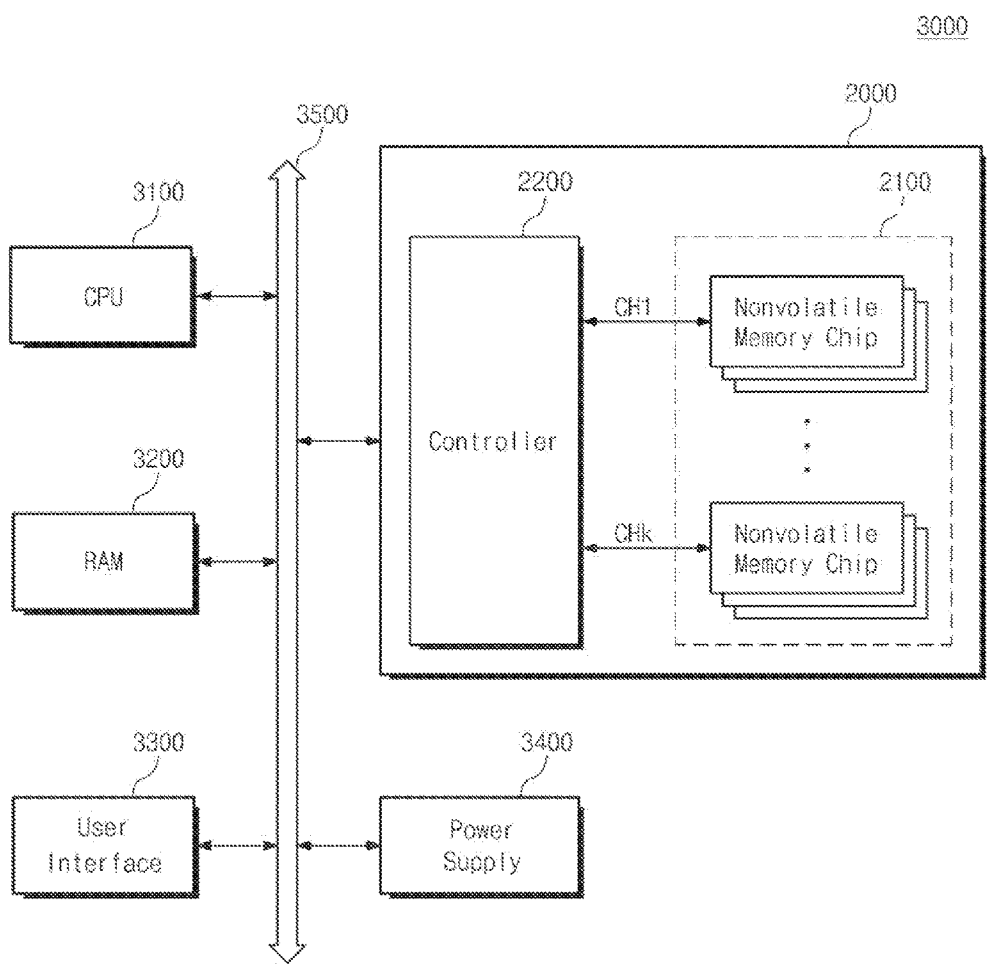

2000
2200
2100
Host
Controller
CH1
CH2
CHk
Nonvolatile Memory Chip
Nonvolatile Memory Chip
Nonvolatile Memory Chip

Fig. 76


3000
2000
3500
2200
2100
3100
CPU
CH1
Nonvolatile Memory Chip
Controller
3200
RAM
CHk
Nonvolatile Memory Chip
3300
User Interface
3400
Power Supply

CONTROL METHOD OF NONVOLATILE MEMORY DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

This U.S. non-provisional patent application is a divisional application of U.S. patent application Ser. No. 13/607,038, filed on Sep. 7, 2012, which is a continuation-in-part claiming priority under 35 U.S.C. §120 to U.S. patent application Ser. No. 13/028,918, filed on Feb. 16, 2011, which claims priority under 35 U.S.C. §119 to Korean Patent Application No. 10-2010-0014271 filed on Feb. 17, 2010 in the Korean Intellectual Property Office (KIPO), Korean Patent Application No. 10-2010-0075065 filed on Aug. 3, 2010 in the Korean Intellectual Property Office (KIPO), and U.S. Provisional Patent Application No. 61/371,431, filed on Aug. 6, 2010. This U.S. non-provisional patent application also claims priority under 35 U.S.C. §119 to Korean Patent Application No. 10-2011-0102017 filed Oct. 6, 2011 in the Korean Intellectual Property Office (KIPO). The entire contents of each of the above-mentioned applications are incorporated by reference herein.

BACKGROUND

The present disclosure herein relates to a semiconductor memory, and more particularly, to a nonvolatile memory device having a 3-dimensional structure, an operating method thereof, and a memory system including the same.

A semiconductor memory device is a memory device that is implemented with semiconductor materials such as silicon (Si), germanium (Ge), gallium arsenide (GaAs) and indium phosphide (InP). Semiconductor memory devices may be largely divided into a volatile memory device and a nonvolatile memory device.

A volatile memory device is a memory device in which stored data are erased when a power source is shut off. Examples of volatile memory devices include Static Random Access Memory (SRAM), Dynamic Random Access Memory (DRAM) and Synchronous Dynamic Random Access Memory (SDRAM). A non-volatile memory device is a memory device that retains stored data even when a power source is shut off. Examples of nonvolatile memory devices include Read-Only Memory (ROM), Programmable Read Only Memory (PROM), Erasable Programmable Read Only Memory (EPROM), Electrical Erasable Programmable Read Only Memory (EEPROM), flash memory devices, Phase-change Random Access Memory (PRAM), Magnetoresistive Random Access Memory (MRAM), Resistive Random Access Memory (RRAM) and Ferroelectric Random Access Memory (FRAM). Flash memory devices may be largely categorized into a NOR type and a NAND type.

SUMMARY

Example embodiments of inventive concepts relate to a control method of a nonvolatile memory device, which includes a plurality of memory blocks on a substrate, each memory block including a plurality of sub blocks stacked in a direction perpendicular to the substrate and being configured to be erased independently and each sub block including a plurality of memory cells stacked in the direction perpendicular to the substrate. The control method includes comparing a count value of a first memory block of the plurality of memory blocks with a reference value, the count value of the first memory block being determined according to the num-

ber of program, read, or erase operations executed at the first memory block after data is programmed in the first memory block; and if the count value of the first memory block is greater than or equal to the reference value, performing a reprogram operation in which data programmed in the first memory block is read and the read data is programmed in a second memory block of plurality of memory blocks.

The control method may further include invalidating the first memory block when the count value of the first memory block is greater than or equal to the reference value.

The control method may further include generating a program, read, or erase command on a sub block of the first memory block before the comparing the count value of the first memory block of the plurality of memory blocks with the reference value; performing a program, read, or erase operation in response to the program, read, or erase command before the comparing the count value of the first memory block of the plurality of memory blocks with the reference value; increasing a count value of the second memory block according to execution of the reprogram operation after the reprogram operation is executed; if the count value is smaller than the reference value, increasing a count value of the first memory block according to the execution of the program, read, or erase operation.

The count value of the first memory block may be increased according to the number of program loops iterated when a program operation is executed.

The count value of the first memory block may be increased according to the number of erase loops iterated when an erase operation is executed.

The count value of the second memory block may be increased according to the number of program and read operations executed at the second memory block when the reprogram operation is executed.

The control method further may include generating a program, read, or erase command on a sub block of the memory block before the comparing the count value of the first memory block of the plurality of memory blocks with the reference value; after the reprogram operation is executed or when the count value of the first memory block is smaller than the reference value, performing a program, read, or erase operation in response to the program, read, or erase command; if the count value of the first memory block is greater than or equal to the reference value after execution of the program, read, or erase operation, increasing a count value of the second memory block according to the reprogram operation and the program, read, or erase operation; and if the count value of the memory block is smaller than the reference value after the execution of the program, read, or erase operation, increasing the count value of the first memory block according to the program, read, or erase operation.

The program, read, or erase command may be an erase command and the count value may be greater than or equal to the reference value, and data programmed in a sub block corresponding to an erase command generated at the reprogram operation may be read inhibited.

The control method may further include generating a program, read, or erase command on a sub block of the first memory block before the comparing the count value of the first memory block of the plurality of memory blocks with the reference value; performing the program, read, or erase operation in response to the program, read, or erase command before the comparing the count value of the first memory block of the plurality of memory blocks with the reference value; increasing the count value of the first memory block according to the program, read, or erase operation before the comparing the count value of the first memory block of the plurality of memory blocks with the reference value; and increasing a count value of the second memory block according to execution of the reprogram operation after the program operation is executed.

Example embodiments of inventive concept relate to a control method of a nonvolatile memory device which includes a plurality of memory blocks on a substrate, each memory block including a plurality of sub blocks stacked in a direction perpendicular to the substrate and being configured to be erased independently and each sub block including a plurality of memory cells stacked in the direction perpendicular to the substrate. The control method includes comparing a count value of program, read, and erase operations, executed at a first memory block after data is programmed in a first sub block of the first memory block of the nonvolatile memory device, with a reference value; and if the count value of the first sub block is over the reference value, reading data programmed in the first sub block to reprogram the read data.

The read data may be reprogrammed in a second sub block of the first memory block.

The read data may be reprogrammed in a sub block of a second memory block of the plurality of memory blocks.

The first sub block may be erased and the read data may reprogrammed in the erased first sub block.

If a count value of the sub block is greater than or equal to the reference value, a count value of the first sub block may be increased when a program, read, or erase operation is performed on the first memory block.

Example embodiments of inventive concept relate to a control method of a nonvolatile memory device which includes a plurality of memory blocks on a substrate, each memory block including a plurality of sub blocks stacked in a direction perpendicular to the substrate and being configured to be erased independently and each sub block including a plurality of memory cells stacked in the direction perpendicular to the substrate. The method includes detecting a count value corresponding to a number of program, read, or erase operations executed at one of a first sub block of a first memory block of the plurality of memory blocks and the first memory block of the plurality of memory blocks after data is programmed in the one of the first sub block of the first memory block of the plurality of memory blocks and the first memory block of the plurality of memory blocks; comparing the detected count value with a reference value; and performing one of a refresh and a reclaim operation when the detected count value is greater than or equal to the reference value.

The count value may correspond to the number of program, read, or erase operations executed at the first sub block of the first memory block after data is programmed in the first sub block of the first memory block of the plurality of memory blocks. The refresh operation may be performed when the detected count value is greater than or equal to the reference value, and the refresh operation may include copying data from the first sub block of the first memory block to at least one sub block of a second memory block of the plurality of memory blocks.

The method may include transmitting a program, read, or erase command to the one of the first sub block of the first memory block of the plurality of memory blocks and the first memory block of the plurality of memory blocks before the comparing the detected count value with the reference value; performing the program, read, or erase operation at the one of the first sub block of the first memory block of the plurality of memory blocks and the first memory block of the plurality of memory blocks in response to the program, read, or erase command; and if the comparing the detected value with the reference value indicates that the detected count value is less than the reference value, increasing the count value corresponding to the one of the first sub block of the first memory block of the plurality of memory blocks and the first memory block of the plurality of memory blocks according to the execution of the program, read, or erase operation.

The method may further include transmitting a program, read, or erase command to the one of the first sub block of the first memory block of the plurality of memory blocks and the first memory block of the plurality of memory blocks after the comparing the detected count value with the reference value; performing the program, read, or erase operation at the one of the first sub block of the first memory block of the plurality of memory blocks and the first memory block of the plurality of memory blocks in response to the program, read, or erase command; and if the comparing the detected value with the reference value indicates that the detected count value is less than the reference value, increasing the count value corresponding to the one of the first sub block of the first memory block of the plurality of memory blocks and the first memory block of the plurality of memory blocks according to the execution of the program, read, or erase operation.

The count value may correspond to the number of program, read, or erase operations executed at the first sub block of the first memory block after data is programmed in the first sub block of the first memory block of the plurality of memory blocks. The reclaim operation may be performed when the detected count value is greater than or equal to the reference value. The reclaim operation may include reading data from the first sub block of the first memory block, erasing the first sub block of the first memory block, and reprogramming the first sub block of the first memory block with the read data. The count value may correspond to the number of program, read, or erase operations executed at the first memory block after data is programmed in the first memory block of the plurality of memory blocks, and the method may further include invalidating the first memory block when the count value of the first memory block is greater than or equal to the reference value.

BRIEF DESCRIPTION OF THE FIGURES

The above and other objects and features will become apparent from the following description with reference to the following figures, wherein like reference numerals refer to like parts throughout the various figures unless otherwise specified, and wherein

FIG. **1** is a block diagram of a memory system **1000** according to example embodiments of inventive concepts;

FIG. **2** is a block diagram of the nonvolatile memory device **100** of FIG. **1**;

FIG. **3** is a block diagram of the memory cell array **110** of FIG. **2**;

FIG. **4** is a perspective view illustrating example embodiments of one memory block BLKi of the memory blocks BLK**1** to BLKz in FIG. **3**;

FIG. **5** is a cross-sectional view taken along line V-V' of the memory block BLKi of FIG. **4**;

FIG. **6** is a cross-sectional view illustrating the transistor structure TS of FIG. **5**;

FIG. **7** is a circuit diagram illustrating an equivalent circuit BLKi_**1** according to example embodiments of the memory block BLKi described with reference to FIGS. **4** to **6**;

FIG. **8** is a circuit diagram illustrating example embodiments in which the memory cells MC of the memory block BLKi_**1** form sub blocks;

FIG. **9** is a table illustrating example embodiments of conditions of voltages which are applied to the memory block BLKi_**1** of FIG. **8** during an erase operation;

FIG. **10** is a timing diagram illustrating voltage variations of the memory block BLKi_**1** according to the voltage conditions of FIG. **9**;

FIG. **11** is a cross-sectional view of one of the NAND strings of the memory block BLKi_**1**;

FIG. **12** is a graph illustrating threshold voltages of the memory cells MC which are measured while varying the first dummy word line voltage Vdwl**1**;

FIG. **13** is a table illustrating example embodiments of conditions of voltages which are applied to the memory block BLKi_**1** of FIG. **8** during an erase operation;

FIG. **14** is a timing diagram illustrating voltage variations of the memory block BLKi_**1** according to the voltage conditions of FIG. **13**;

FIG. **15** is a cross-sectional view of one of the NAND strings of the memory block BLKi_**1**;

FIG. **16** is a diagram illustrating example embodiments of the threshold voltage distribution of the memory cells MC of the memory block BLKi_**1** in FIG. **8**;

FIG. **17** is a diagram illustrating example embodiments of the threshold voltage distribution of the memory cells MC of the memory block BLKi_**1** in FIG. **8**;

FIG. **18** is a flowchart illustrating a refresh method according to example embodiments of inventive concepts;

FIG. **19** is a block diagram illustrating a flash translation layer **600** driven in the controller of FIG. **1**;

FIG. **20** is a flow chart illustrating a method of operating the refresh unit **630** of FIG. **19**;

FIG. **21** is a block diagram schematically illustrating a flash translation layer driven by a controller in FIG. **1** according to example embodiments of inventive concepts;

FIG. **22** is a flowchart illustrating a control method of controlling a nonvolatile memory device via a flash translation layer in FIG. **21**;

FIG. **23** is a flowchart for describing a control method of FIG. **22** according to example embodiments of inventive concepts;

FIGS. **24** and **25** are flowcharts for describing a control method of FIG. **22** according to example embodiments of inventive concepts;

FIG. **26** is a flowchart for describing a control method of FIG. **22** according to example embodiments of inventive concepts;

FIG. **27** is a flowchart for describing an operation of increasing a count value of a memory block according to example embodiments of inventive concepts;

FIG. **28** is a flowchart for describing an operation of increasing a count value of a memory block according to example embodiments of inventive concepts;

FIG. **29** is a flowchart for describing an operation of increasing a count value of a memory block according to example embodiments of inventive concepts;

FIG. **30** is a flowchart for describing a control method of FIG. **22** according to example embodiments of inventive concepts;

FIG. **31** is a flowchart for describing a control method of FIG. **22** according to example embodiments of inventive concepts;

FIG. **32** is a flowchart for describing a control method of FIG. **22** according to example embodiments of inventive concepts;

FIG. **33** is a flowchart for describing a control method of FIG. **22** according to example embodiments of inventive concepts;

FIG. **34** is a flowchart for describing a control method of FIG. **22** according to example embodiments of inventive concepts;

FIG. **35** is a flowchart for describing a control method of FIG. **22** according to example embodiments of inventive concepts;

FIG. **36** is a flowchart for describing a control method of FIG. **22** according to example embodiments of inventive concepts;

FIG. **37** is a flowchart for describing a control method of FIG. **22** according to example embodiments of inventive concepts;

FIG. **38** is a circuit diagram schematically illustrating sub blocks, formed of memory cells in a memory block in FIG. **7**, according to example embodiments of inventive concepts;

FIG. **39** is a perspective view illustrating one of the memory blocks BLK**1** to BLKz of FIG. **3** according to example embodiments of inventive concepts;

FIG. **40** is a sectional view taken along the line XL-XL' of a memory block of FIG. **39**;

FIG. **41** is a circuit diagram illustrating an equivalent circuit of the memory block BLKj described with reference to FIGS. **39** and **40**;

FIG. **42** is a table illustrating voltage conditions applied to the memory block BLKj_**1** of FIG. **41** during an erase operation;

FIG. **43** is a timing diagram illustrating a voltage change of the memory block BLKj_**1** of FIG. **41** according to a voltage condition of FIG. **42**;

FIG. **44** is a sectional view illustrating one NAND string of the memory block BLKj_**1**;

FIG. **45** is a perspective view illustrating one among the memory blocks BLK**1** to BLKz of FIG. **3** according to example embodiments of inventive concepts;

FIG. **46** is a sectional view taken along the line III-III' of the memory block BLKm of FIG. **45**;

FIG. **47** is a sectional view illustrating one NAND string NS of the memory block BLKm;

FIG. **48** is a perspective view illustrating one among the memory blocks BLK**1** to BLKz of FIG. **3** according to example embodiments of inventive concepts;

FIG. **49** is a sectional view taken along the line IV-IV' of the memory block BLKn of FIG. **48**;

FIG. **50** is a circuit diagram illustrating an equivalent circuit BLKi_**2** of the memory block BLKi described with reference to FIGS. **4** and **6** according to example embodiments of inventive concepts;

FIG. **51** is a circuit diagram illustrating an equivalent circuit BLKi_**3** of the memory block BLKi described with reference to FIGS. **4** and **6** according to example embodiments of inventive concepts;

FIG. **52** is a circuit diagram illustrating an equivalent circuit BLKi_**4** of the memory block BLKi described with reference to FIGS. **4** and **6** according to example embodiments of inventive concepts;

FIG. **53** is a circuit diagram illustrating an equivalent circuit BLKi_**5** of the memory block BLKi described with reference to FIGS. **4** and **6** according to example embodiments of inventive concepts;

FIG. **54** is a circuit diagram illustrating an equivalent circuit BLKi_**6** of the memory block BLKi described with reference to FIGS. **4** and **6** according to example embodiments of inventive concepts;

FIG. **55** is a circuit diagram illustrating an equivalent circuit BLKi_**7** of the memory block BLKi described with reference to FIGS. **4** and **6** according to example embodiments of inventive concepts;

FIG. **56** is a circuit diagram illustrating an equivalent circuit BLKi_**8** of the memory block BLKi described with reference to FIGS. **4** and **6** according to example embodiments of inventive concepts;

FIG. **57** is a perspective view of one of the memory blocks BLK**1**-BLKz according to example embodiments of inventive concepts;

FIG. **58** is a cross-sectional view taken along the line V-V' of the memory block BLKo of FIG. **57**;

FIG. **59** is a perspective view of one of the memory blocks BLK**1**-BLKz according to example embodiments BLKi' of inventive concepts;

FIG. **60** is a perspective view of one of the memory blocks BLK**1**-BLKz according to example embodiments of inventive concepts;

FIG. **61** is a perspective view of one of the memory blocks BLK**1**-BLKz according to example embodiments BLKp of inventive concepts;

FIG. **62** is a sectional view taken along the line LVII-LXII' of the memory block BLKp of FIG. **61**;

FIG. **63** is a table illustrating example embodiments of voltage conditions during an erase operation of the memory block BLKp of FIGS. **61** and **62**;

FIG. **64** is a timing diagram illustrating a voltage change of the memory block BLKp of FIGS. **61** and **62** according to the voltage conditions of FIG. **63**;

FIG. **65** is a table illustrating voltage conditions when dummy memory cells DMC are not provided between sub blocks of the memory block BLKp of FIGS. **43** and **44**;

FIG. **66** is a timing diagram illustrating a voltage change according to the voltage conditions of FIG. **65**;

FIG. **67** is a perspective view of one of the memory blocks BLK**1**-BLKz according to example embodiments of inventive concepts;

FIG. **68** is a sectional view taken along the line LXVIII-LXVIII' of the memory block BLKq of FIG. **61**;

FIG. **69** is a perspective view of one of the memory blocks BLK**1**-BLKz according to example embodiments of inventive concepts;

FIG. **70** is a sectional view taken along the line LXX-LXX' of the memory block BLKr of FIG. **69**;

FIG. **71** is a perspective view of one of the memory blocks BLK**1**-BLKz according to example embodiments of inventive concepts;

FIG. **72** is a sectional view taken along the line LXXII-LXXII' of the memory block BLKs of FIG. **71**;

FIG. **73** is a perspective view of one of the memory blocks BLK**1**-BLKz according to example embodiments of inventive concepts;

FIG. **74** is a sectional view taken along the line LXXIV-LXXIV' of the memory block BLKt of FIG. **73**;

FIG. **75** is a block diagram illustrating an application example of the memory system **1000** of FIG. **1**; and

FIG. **76** is a block diagram illustrating a computing system **3000** with the memory system **2000** described with reference to FIG. **75**.

DETAILED DESCRIPTION

The inventive concept is described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the inventive concept are shown. This inventive concept may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the inventive concept to those skilled in the art. In the drawings, the size and relative sizes of layers and regions may be exaggerated for clarity. Like numbers refer to like elements throughout.

It will be understood that, although the terms first, second, third etc. may be used herein to describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one element, component, region, layer or section from another region, layer or section. Thus, a first element, component, region, layer or section discussed below could be termed a second element, component, region, layer or section without departing from the teachings of the inventive concept.

Spatially relative terms, such as "beneath", "below", "lower", "under", "above", "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. It will be understood that the spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. For example, if the device in the figures is turned over, elements described as "below" or "beneath" or "under" other elements or features would then be oriented "above" the other elements or features. Thus, the exemplary terms "below" and "under" can encompass both an orientation of above and below. The device may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein interpreted accordingly. In addition, it will also be understood that when a layer is referred to as being "between" two layers, it can be the only layer between the two layers, or one or more intervening layers may also be present.

The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the inventive concept. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

It will be understood that when an element or layer is referred to as being "on", "connected to", "coupled to", or "adjacent to" another element or layer, it can be directly on, connected, coupled, or adjacent to the other element or layer, or intervening elements or layers may be present. In contrast, when an element is referred to as being "directly on," "directly connected to", "directly coupled to", or "immediately adjacent to" another element or layer, there are no intervening elements or layers present.

Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this inventive concept belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and/or the present specification and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

The term "selected memory block" may be used to indicate a memory block, selected for programming, erasing, or reading, from among a plurality of memory blocks. The term "selected sub block" may be used to indicate a sub block, selected for programming, erasing, or reading, from among a plurality of sub blocks in one memory block.

The term "selected bit line" or "selected bit lines" may be used to indicate a bit line or bit lines, connected with a cell transistor to be programmed or read, from among a plurality of bit lines. The term "unselected bit line" or "unselected bit lines" may be used to indicate a bit line or bit lines, connected with a cell transistor to be program-inhibited or read-inhibited, from among a plurality of bit lines.

The term "selected string selection line" may be used to indicate a string selection line, connected with a cell string including a cell transistor to be programmed or read, from among a plurality of string selection lines. The term "unselected string selection line" or "unselected string selection lines" may be used to indicate a remaining string selection line or remaining string selection lines other than the selected string selection line from among a plurality of string selection lines. The term "selected string selection transistors" may be used to indicate string selection transistors connected with a selected string selection line. The term "unselected string selection transistors" may be used to indicate string selection transistors connected with an unselected string selection line or unselected string selection lines.

The term "selected ground selection line" may be used to indicate a ground selection line, connected with a cell string including a cell transistor to be programmed or read, among a plurality of ground selection lines. The term "unselected ground selection line" may be used to indicate a remaining ground selection line or remaining ground selection lines other than the selected ground selection line from among a plurality of ground selection lines. The term "selected ground selection transistors" may be used to indicate ground selection transistors connected with a selected ground selection line. The term "unselected ground selection transistors" may be used to indicate ground selection transistors connected with an unselected ground selection line or unselected ground selection lines.

The term "unselected word line" may be used to indicate a word line, connected with a cell transistor to be programmed or read, from among a plurality of word lines. The term "unselected word line" or "unselected word lines" may be used to indicate a remaining word lines or remaining word lines other than a selected word line from among a plurality of word lines.

The term "selected memory cell" or "selected memory cells" may be used to designate memory cells to be programmed or read among a plurality of memory cells. The term "unselected memory cell" or "unselected memory cells" may be used to indicate a remaining memory cell or remaining memory cells other than a selected memory cell or selected memory cells from among a plurality of memory cells.

Embodiments of the inventive concept will be described with reference to a NAND flash memory. However, the inventive concept is not limited thereto. The inventive concept may be applied to nonvolatile memory devices such as an Electrically Erasable and Programmable ROM (EEPROM), a NOR flash memory, a Phase-change RAM (PRAM), a Magnetic RAM (MRAM), a Resistive RAM (RRAM), a Ferroelectric RAM (FRAM), and the like.

FIG. **1** is a block diagram of a memory system **1000** according to example embodiments of inventive concepts. Referring to FIG. **1**, the memory system **1000** includes a nonvolatile memory device **100** and/or a controller **500**.

The nonvolatile memory device **100** has a configuration allowing data to be stored therein. The nonvolatile memory device will be described in more detail with reference to FIG. **2**.

The controller **500** is connected to a host and a nonvolatile memory device **100**. In response to a request from the host, the controller **500** is configured to access the nonvolatile memory device **100**. For example, the controller **500** is configured to control read, write, erase and perform background operations of the nonvolatile memory device **100**. The controller **500** is configured to provide an interface between the nonvolatile memory device **100** and the host. The controller **500** is configured to drive a firmware controlling the nonvolatile memory device **100**.

The controller **500** includes an internal bus **510**, a processor **520**, a random access memory (RAM) **530**, a host interface **540**, an error correction block **550**, and/or a memory interface **560**.

The internal bus **510** provides a channel between elements of the controller **500**.

The processor **520** is configured to control the overall operation of the controller **500**. The processor **520** is configured to drive firmware, code, etc. which are driven in the controller **500**. For example, the processor **520** is configured to drive firmware, code, etc., that control the nonvolatile memory device **100**.

The RAM **530** is used as at least one of an operating memory, a cache memory between the nonvolatile memory device **100** and the host, and a buffer memory between the nonvolatile memory device **100** and the host.

The host interface **540** includes a protocol performing data exchange between the host and the controller **500**. For example, the host interface **540** is configured to communicate with an external device (host) through at least one of various interface protocols such as a universal serial bus (USB) protocol, a multimedia card (MMC) protocol, a peripheral component interconnection (PCI) protocol, a PCI-express (PCI-E) protocol, an advanced technology attachment (ATA) protocol, a serial-ATA protocol, a parallel-ATA protocol, a small computer small interface (SCSI) protocol, an enhanced small disk interface (ESDI) protocol, and an integrated drive electronics (IDE) protocol.

The error correction block **550** includes an error correcting code (ECC). The error correction block **550** detects an error in data read from the nonvolatile memory device **100** by use of the ECC, and corrects the error.

The memory interface **560** interfaces with the nonvolatile memory device **100**. For example, the memory interface includes a NAND interface and/or NOR interface.

The controller **500** and the nonvolatile memory device **100** may be integrated into a single semiconductor device. For example, the controller **500** and the nonvolatile memory device **100** are integrated into a single semiconductor device, and form a memory card. For instance, the controller **500** and the nonvolatile memory device **100** are integrated into a single semiconductor device to thereby form a memory card such as a PC card (PCMCIA, personal computer memory card international association), a compact flash card (CF), a smart media card (SM, SMC), a memory stick, a multimedia card (MMC, RS-MMC, MMCmicro), an SD card (SD, miniSD, microSD, SDHC), and a universal flash storage (UFS).

The controller **500** and the nonvolatile memory device **100** are integrated into a single semiconductor device to thereby form a semiconductor drive such as solid state drive (SSD). The SSD includes a storage unit configured to store data in a semiconductor memory. In the case where the memory system **1000** is used as the SSD, the operating speed of the host connected to the memory system **1000** may be improved.

As another example, the memory system **1000** may be provided as one of various components of an electronic device such as a computer, a ultra mobile personal computer (UMPC), a workstation, a net-book, a personal digital assistance (PDA), a portable computer (PC), a web tablet, a wireless phone, a mobile phone, a smart phone, an e-book, a portable multimedia player (PMP), a portable game console, a navigation device, a black box, a digital camera, a digital multimedia broadcasting (DMB) player, a digital audio recorder, a digital audio player, a digital picture recorder, a digital picture player, a digital video recorder, a digital video player, a device for transmitting and receiving information in a wireless environment, one of various electronic devices constituting a home network, one of various electronic devices constituting a computer network, one of various electronic devices constituting a telematics network, a radio frequency identification (RFID) device, and one of various components constituting a computing system.

The nonvolatile memory device **100** or the memory system **1000** may be implemented using various kinds of packages. For instance, the nonvolatile memory device **100** or the memory system **1000** may be implemented with packages such as Package on Package (PoP), Ball Grid Arrays (BGA), Chip Scale Packages (CSP), Plastic Leaded Chip Carrier (PLCC), Plastic Dual In-line Package (PDIP), Die in Waffle Pack, Die in Wafer Form, Chip On Board (COB), Ceramic Dual In-line Package (CERDIP), Plastic Metric Quad Flat Pack (MQFP), Thin Quad Flat Pack (TQFP), Small Outline Integrated Circuit (SOIC), Shrink Small Outline Package (SSOP), Thin Small Outline Package (TSOP), System In Package (SIP), Multi Chip Package (MCP), Wafer-level Fabricated Package (WFP), and Wafer-level Processed Stack Package (WSP).

FIG. **2** is a block diagram of the nonvolatile memory device **100** of FIG. **1**. Referring to FIG. **1**, the nonvolatile memory device **100** includes a memory cell array **110**, an address decoder **120**, a read & write circuit **130**, a data input/output (I/O) circuit **140**, and/or a control logic **150**.

The memory cell array **110** is connected to the address decoder **120** through word lines WL and select lines SL, and connected to the read & write circuit **130** through bit lines BL. The memory cell array **110** includes a plurality of memory cells. For example, the memory cell array **100** includes a plurality of memory cells which are stacked in a direction vertical to a substrate. For instance, the memory cell array **110** includes a plurality of memory cells each of which can store one or more bit(s) therein.

The address decoder **120** is connected to the memory cell array **110** through the word lines WL and the select lines SL. The address decoder **120** is configured to operate in response to the control of the control logic **150**. The address decoder **120** receives addresses ADDR from an external device.

The address decoder **120** is configured to decode a row address of the received addresses ADDR. The address decoder **120** selects a word line corresponding to the decoded row address among the word lines WL. The address decoder **120** selects a select line corresponding to the decoded row address among the select lines SL.

When the address decoder **120** is additionally connected to the memory cell array **110** through dummy word lines DWL (not shown), the address decoder **120** may further select a dummy word line corresponding to the decoded row address among the dummy word lines DWL (not shown).

The address decoder **120** is configured to decode a column address of the received addresses ADDR. The address decoder **120** transfers the decoded column address to the read & write circuit **130**.

For example, the address decoder **120** may include a row decoder decoding a row address, a column address decoding a column address, and an address buffer storing the received address ADDR.

The read & write circuit **130** is connected to the memory cell array **110** through bit lines BL, and connected to the data I/O circuit **140** through data lines DL. The read & write circuit **130** operates in response to the control of the control logic **150**. The read & write circuit **130** receives the decoded column address from the address decoder **120**. The read & write circuit **130** selects bit lines BL using the decided column address.

The read & write circuit **130** receives data from the data I/O circuit **140**, and writes the received data to the memory cell array. The read & write circuit **130** reads data from the memory cell array, and transfers the read data to the data I/O circuit **140**. The read & write circuit **130** reads data from a first storage region of the memory cell array **110**, and writes the read data to a second storage region of the memory cell array **110**. For instance, the read & write circuit performs a copy-back operation.

The read & write circuit **130** may include elements such as a page buffer (or page register) and/or a column select circuit. In another example, the read & write circuit **130** may include elements such as a sense amplifier, a write driver, and/or a column select circuit.

The data I/O circuit **140** is connected to the read & write circuit through the data lines DL. The data I/O circuit **140** operates in response to the control of the control logic **140**. The data I/O circuit **140** is configured to exchange data DATA with an external device. The data I/O circuit **140** is configured to transfer the data DATA transferred from the external device to the read & write circuit **130** through the data lines DL. The data I/O circuit **140** is configured to output the data DATA transferred through the data lines DL from the read & write circuit **130** to the external device. Exemplarily, the data I/O circuit **140** may include an element such as a data buffer.

The control logic **150** is connected to the address decoder **120**, the read & write circuit **130**, and the data I/O circuit **140**. The control logic **150** is configured to control the overall operation of the nonvolatile memory device **100**. The control logic **150** operates in response to a control signal CTRL transferred from the external device.

The control logic **150** includes a voltage generator **151**. For example, the voltage generator **151** is configured to generate a plurality of voltages including a high voltage. For example, one of the voltages generated by the voltage generator **151** is applied to the word lines WL through the address decoder **120**. When dummy word lines DWL (not shown) are additionally provided in the memory cell array **110**, one of the voltage generated by the voltage generator **151** may be further transferred to the dummy word lines DWL (not shown).

One of the voltages generated by the voltage generator **151** may be transferred to the memory cell array **110**. For example, one of the voltages generated by the voltage generator **151** may be transferred to the substrate of the memory cell array **110**.

FIG. **3** is a block diagram of the memory cell array **110** of FIG. **2**. Referring to FIG. **3**, the memory cell array **110** includes a plurality of memory blocks BLK**1** to BLKz. Each of the memory blocks BLK has a three dimensional structure (or vertical structure). For example, each memory block BLK includes structures extending in first to third directions. For instance, each memory block BLK includes a plurality of NAND strings NS extending in the second direction. For example, a plurality of NAND strings NS may be provided in the first and third directions, for example, in a two-dimensional array of NAND strings NS.

Each NAND string NS is connected to a bit line BL, a string select line SSL, a ground select line GSL, the word lines WL, and a common source line CSL. Each of the memory blocks is connected to the plurality of bit lines BL, the plurality of string select lines SSL, the plurality of ground select lines GSL, the plurality of word lines WL, and the common source line CSL. The memory blocks BLK**1** to BLKz will be more fully described with reference to FIG. **4**.

The memory blocks BLK**1** to BLKz are selected by the address decoder **120** illustrated in FIG. **2**. For instance, the address decoder **120** is configured to select at least one memory block BLK corresponding to the decoded row address among the memory blocks BLK**1** to BLKz.

FIG. **4** is a perspective view illustrating example embodiments of one memory block BLKi of the memory blocks BLK**1** to BLKz in FIG. **3**. FIG. **5** is a cross-sectional view taken along line V-V' of the memory block BLKi of FIG. **4**. Referring to FIGS. **4** and **5**, the memory block BLKi includes structures extending in the first to third directions.

First, a substrate **111** is provided. The substrate **111** may be a well having a first type (e.g., first conductive type). For example, the substrate **111** may be a p-type well formed by implanting Group III elements such as boron (B). For example, the substrate **111** is a p-type pocket well provided in an n-type well. Hereinafter, it is assumed that the substrate **111** be a p-type well (or p-type pocket well). However, the conductive type of the substrate **111** is not limited to the p-type well.

A plurality of doping regions **311** to **314** extending in a first direction are provided on the substrate **111**. For example, the plurality of doping regions **311** to **314** may have a second type (e.g., second conductive type) differing from that of the substrate **111**. Hereinafter, it is assumed that the first to fourth doping regions **311** to **314** have an n-type. However, the conductive types of the first to fourth doping regions **311** to **314** are not limited to the n-type.

A plurality of insulation materials **112** extending in the first direction are sequentially provided in a second direction over a region of the substrate **111** between the first and second doping regions **311** and **312**. For example, the plurality of insulation materials **112** may be provided in the second direction such that they are spaced by a predetermined or desired distance. The insulation material **112** may include an insulator such as silicon oxide.

A plurality of pillars **113** are provided, which are disposed in the first direction on the region of the substrate **111** between the first and second doping regions **311** and **312** and penetrate the insulation materials **112** in the second direction. Exemplarily, the plurality of pillars **113** penetrate the insulation materials **112** to contact the substrate **111**.

Each of the pillars **113** may be composed of a plurality of materials. For instance, a surface layer **114** of each pillar **113** may include a silicon material having a first type. For example, the surface layer **114** of each pillar **113** may include a silicon material having the same type as the substrate **111**. Hereinafter, it is assumed that the surface layer **114** of each pillar **113** includes p-type silicon. However, the surface layer **114** of each pillar **113** is not limited to including p-type silicon.

An inner layer **115** of each pillar **113** is composed of an insulation material. For example, the inner layer **115** of each pillar **113** may include an insulation material such as silicon oxide. For example, the inner layer **115** of each pillar **113** may include an air gap. Also a void may be formed in the inner layer **115**.

In a region between the first and second doping regions **311** and **312**, an insulation layer **116** is provided along exposed surfaces of the insulation materials **112**, the pillars **113**, and the substrate **111**. Exemplarily, the insulation layer **116** provided on the exposed side of the last insulation material **112** disposed in the second direction may be removed along the second direction.

For example, the thickness of the insulation material **116** may be less than a half of the distance between the insulation materials **112**. That is, a region, in which any material other than the insulation materials **112** and the insulation layer **116** may be disposed, may be provided between the insulation layer **116** provided on an undersurface of the first insulation material and the insulation layer **116** provided on a top surface of the second insulation material under the first insulation material of the insulation material **112**.

In the region between the first and second doping regions **311** and **312**, first conductive materials **211** to **291** are provided on an exposed surface of the insulation layer **116**. For example, the first conductive material **211** extending in the first direction is provided between the substrate **111** and the insulation layer adjacent thereto. More specifically, the first conductive material **211** extending in the first direction is provided between the substrate **111** and the insulation layer **116** disposed under the insulation material **112** adjacent to the substrate **111**. Between the insulation layer **116** on a top surface of a specific insulation material and the insulation layer disposed on an undersurface of an insulation layer provided on top of the specific insulation material among the insulation materials **112**, the first conductive material extending in the first direction is provided. Exemplarily, a plurality of first conductive materials **221** to **281** extending in the first direction are provided between the insulation materials **112**. Exemplarily, the first conductive materials **211** to **291** may be a metallic material. Exemplarily, the first conductive materials **211** to **291** may be a conductive material such as polysilicon.

A structure identical to a structure disposed on the first and second doping regions **311** and **312** is provided in a region between the second and third doping regions **312** and **313**. Exemplarily, the plurality of insulation materials **112** extending in the first direction, the plurality of pillars **113** which are sequentially arranged in the first direction and penetrate the plurality of insulation materials **113** in the third direction, the insulation layer **116** provided on the plurality of insulation materials **112** and the exposed surface of the plurality of pillars **112**, and the plurality of first conductive materials **212** to **292** extending in the first direction are provided in the region between the second and third doping regions **312** and **313**.

A structure identical to a structure disposed on the first and second doping regions **311** and **312** is provided in a region between the third and fourth doping regions **313** and **314**. Exemplarily, the plurality of insulation materials **112** extending in the first direction, the plurality of pillars **113** which are sequentially arranged in the first direction and penetrate the plurality of insulation materials **113** in the third direction, the insulation layer **116** provided on the plurality of insulation materials **112** and the exposed surface of the plurality of pillars **112**, and the plurality of first conductive materials **213** to **293** extending in the first direction are provided in the region between the third and fourth doping regions **313** and **314**.

Drains **320** are respectively provided on the plurality of pillars **113**. Exemplarily, the drains **320** may include a silicon material doped with a second type material. For example, the drains **320** may include a silicon material doped with an n-type material. Hereinafter, it is assumed that the drains **320** include a silicon material doped with an n-type material. However, the drains **320** are not limited to including n-type silicon materials.

Exemplarily, the width of each drain **320** may be greater than the width of the pillar **113** corresponding thereto. For example, each drain **320** may be provided in the shape of a pad on the top surface of the corresponding pillar **113**. Exemplarily, each of the drains **320** may extend up to a portion of the surface layer **114** of the corresponding pillar **113**.

Second conductive materials **331** to **333** extending in the third direction are provided on the drains **320**. The second conductive materials **331** to **333** are arranged in the first direction such that they are spaced apart from each other by a predetermine or desired distance. The second conductive materials **331** to **333** are respectively connected to the drains **320** in the corresponding region. Exemplarily, the drains **320** and the second conductive material **333** extending in the third direction may be connected to each other through respective contact plugs. Exemplarily, the second conductive materials **331** to **333** may be a metallic material. Exemplarily, the second conductive materials **331** to **333** may be a conductive material such as polysilicon.

Hereinafter, heights of the first conductive materials **211** to **291**, **212** to **292**, and **213** to **293** will be defined. The first conductive materials **211** to **291**, **212** to **292**, and **213** to **293** are defined to have first to ninth heights from the substrate **111** sequentially. That is, the first conductive materials **211** to **213** adjacent to the substrate **111** have the first height. The first conductive materials **291** to **293** adjacent to the second conductive materials **331** to **333** have the ninth height. As an order of the specific conductive materials of the first conductive materials **211** to **291**, **212** to **292**, and **213** to **293** increases from the substrate **111**, the height of the first conductive material increases.

In FIGS. **4** and **5**, each of the pillars **113** forms a string together with the insulation layer **116** and the plurality of first conductive materials **211** to **291**, **212** to **292**, and **213** to **293**. For example, each pillar **113**, acting as a common active pillar, forms a NAND string NS together with a region adjacent to the insulation layer **116** and an adjacent region of the first conductive materials **211** to **291**, **212** to **292**, and **213** to **293**. The NAND string NS includes a plurality of transistor structures TS. The transistor structure TS will be more fully described with reference to FIG. **6**. In example embodiments, a subset of the plurality of transistor structures TS in any given string may be referred to as a substring.

FIG. **6** is a cross-sectional view illustrating the transistor structure TS of FIG. **5**. Referring to FIGS. **4** to **6**, the insulation layer **116** includes first to third sub insulation layers **117**, **118** and **119**. The surface layer **114** of the pillar **113** containing p-type silicon may act as a body. The first sub insulation layer **117** adjacent to the pillar **113** may act as a tunneling insulation layer. For example, the first sub insulation layer **117** adjacent to the pillar **113** may include a thermal oxide layer.

The second sub insulation layer **118** may act as a charge storage layer. For example, the second sub insulation layer **118** may act as a charge trap layer. For example, the second sub insulation layer **118** may include a nitride layer or a metal oxide layer (e.g., aluminum oxide layer, hafnium oxide layer, etc.).

The third sub insulation layer **119** adjacent to the first conductive material **233** may act as a blocking insulation layer. Exemplarily, the third sub insulation layer **119** adjacent to the first conductive material **133** extending in the first direction may have a mono-layered or multi-layered structure. The third sub insulation layer **119** may be a high dielectric layer (e.g., aluminum oxide layer, hafnium oxide layer, etc.) having a higher dielectric constant than the first and second sub insulation layers **117** and **118**.

The first conductive material **233** may act as a gate (or control gate). That is, the first conductive material **233** acting as the gate (or control gate), the third sub insulation layer **119** acting as the blocking insulation layer, the second sub insulation layer **118** acting as the charge trap layer, the first sub insulation layer **117** acting as the tunneling insulation layer, and the surface layer **114** that contains p-type silicon and acts as the body, may form a transistor (or memory cell transistor structure). Exemplarily, the first to third sub insulation layers **117** to **119** may form an ONO structure (oxide-nitride-oxide). Hereinafter, the surface layer **114** of the pillar **113** containing p-type silicon is defined to act as the body in the second direction. In example embodiments, the angles between layers of the pillar **113**, the insulation layer **116**, and the first conductive material **233** may be right angles, acute angles or obtuse angles.

In the memory block BLKi, one pillar **113** corresponds to one NAND string NS. The memory block BLKi includes the plurality of pillars **113**. That is, the memory block BLKi includes the plurality of NAND strings NS. More specifically, the memory block BLKi includes a plurality of NAND strings NS extending in the second direction (or direction perpendicular to the substrate).

Each of the NAND strings NS includes the plurality of transistor structures TS which are stacked in the second direction. At least one of the plurality of transistor structures TS of each NAND string NS acts as a string select transistor SST. At least one of the plurality of transistor structures TS of each NAND string acts as a ground select transistor GST. In example embodiments, a substring of the plurality of transistor structures TS may omit the string select transistor SST and/or the ground select transistor GST.

The gates (or control gates) correspond to the first conductive materials **211** to **291**, **212** to **292**, and **213** to **293** extending in the first direction. That is, the gates (or control gates) form word lines WL extending in the first direction, and at least two select lines SL (for example, at least one string select line SSL and at least one ground select line GSL).

The second conductive materials **331** to **333** extending in the third direction are connected to one ends of the NAND strings NS. For example, the second conductive materials **331** to **333** extending in the third direction act as bit lines BL. That is, in one memory block BLKi, one bit line BL is connected to the plurality of NAND strings.

The second type doping regions **311** to **314** extending in the first direction are provided at the other ends of the NAND strings NS. The second type doping regions **311** to **314** extending in the first direction act as a common source line CSL.

In summary, the memory block BLKi includes the plurality of NAND strings NS extending in a direction (second direction) perpendicular to the substrate **111**, and operate as a NAND flash memory block (e.g., charge trap type) in which the plurality of NAND strings NS are connected to one bit line BL.

In FIGS. **4** to **6**, it has been described that the first conductive materials **211** to **291**, **212** to **292**, and **213** to **293** are provided on nine layers. However, the first conductive materials **211** to **291**, **212** to **292**, and **213** to **293** are not limited to being provided on the nine layers. For example, the first conductive materials may be provided upon at least eight layers forming memory cells, and at least two layers forming select transistors. Also, the first conductive materials may be provided upon a plurality of layers forming memory cells, and at least two layers forming select transistors. For example, the first conductive materials may also be provided on a layer forming dummy memory cells.

In FIGS. **4** to **6**, it has been described that three NAND strings NS are connected to one bit line BL. However, it is not limited that three NAND strings NS are connected to one bit line BL. Exemplarily, m number of NAND strings NS may be connected to one bit line BL in the memory block BLKi. Here, the number of the first conductive materials **211** to **291**, **212** to **292**, and **213** to **293** extending in the first direction, and the number of doping regions **311** to **314** acting as the common source line CSL may also be adjusted so as to correspond to the number of NAND strings NS connected to one bit line BL.

In FIGS. **4** to **6**, it has been described that three NAND strings NS are connected to one of the first conductive materials extending in the first direction. However, it is not limited that three NAND strings NS are connected to one of the first conductive materials. For example, n number of NAND strings NS may be connected to one of the first conductive materials. Here, the number of the second conductive materials **331** to **333** extending in the third direction may also be adjusted to correspond to the number of NAND strings NS connected to one of the first conductive materials.

As illustrated in FIGS. **4** to **6**, a sectional area of the pillar **113** in the first and third directions may be smaller as the pillar **113** gets closer to the substrate **111**. For example, the sectional area of the pillar **113** in the first and third directions may be varied due to process characteristics or errors.

Exemplarily, the pillar **113** is formed by filling a material such as silicon and insulating materials into a hole formed by etching. As the etched depth is greater, an area of the hole in the first and third directions which is formed by etching may be smaller. That is, the sectional area of the pillar **113** in the first and third directions may be smaller as the pillar **113** gets closer to the substrate **111**.

FIG. **7** is a circuit diagram illustrating an equivalent circuit BLKi_**1** according to example embodiments of the memory block BLKi described with reference to FIGS. **4** to **6**. Referring to FIGS. **4** to **7**, NAND strings NS**11** to NS**31** are provided between a first bit line BL**1** and a common source line CSL. NAND strings NS**12**, NS**22** and NS**32** are provided between a second bit line BL**2** and the common source line CSL. NAND strings NS**13**, NS**23** and NS**33** are provided between a third bit line BL**3** and the common source line CSL. The first to third bit lines BL**1** to BL**3** respectively correspond to the second conductive materials **331** to **333** extending in the third direction.

A string select transistor SST of each NAND string NS is connected to the corresponding bit line BL. A ground select transistor GST of each NAND string NS is connected to the common source line CSL. Memory cells MC are provided between the string select transistor SST and the ground select transistor GST of each NAND string NS.

Hereinafter, the NAND strings NS are defined in units of rows and columns. The NAND strings NS commonly connected to one bit line form one column. For example, the NAND strings NS **11** to NS **31** connected to the first bit line BL**1** correspond to a first column. The NAND strings NS**12** to NS **32** connected to the second bit line BL**2** correspond to a second column. The NAND strings NS**13** to NS **33** connected to the third bit line BL**3** correspond to a third column.

The NAND strings NS connected to one string select line SSL form one row. For example, the NAND strings NS **11** to NS**13** connected to the first string select line SSL**1** form a first row. The NAND strings NS**21** to NS**23** connected to the second string select line SSL**2** form a second row. The NAND strings NS**31** to NS**33** connected to the third string select line SSL**3** form a third row.

A height is defined in each NAND string NS. Exemplarily, the height of the ground select transistor GST is defined as 1 in each NAND string NS. The height of the memory cell MC**1** adjacent to the ground select transistor GST is defined as 2. The height of the string select transistor SST is defined as 9. The height of the memory cell MC**6** adjacent to the string select transistor SST is defined as 8.

As an order of the memory cell MC increases from the ground select transistor GST, the height of the memory cell MC increases. That is, first to third memory cells MC**1** to MC**3** are defined to have second to fourth heights, respectively. A dummy memory cell is defined to have a fifth height. Fourth to sixths memory cells MC**4** to MC**6** are defined to have sixth to eighth heights, respectively.

The NAND strings NS of the same row share the ground select line GSL. The NAND strings NS arranged in different rows share the ground select line GSL. The first conductive materials **211** to **213** having the first height are connected to each other to thereby form the ground select line GSL.

The memory cells MC having the same height in the NAND strings NS of the same row share the word line WL. The word lines WL of the NAND strings NS which have the same height and correspond to different rows are commonly connected. That is, the memory cells MC with the same height share the word line WL.

The first conductive materials **221** to **223** having the second height are commonly connected to form the first word line WL**1**. The first conductive materials **231** to **233** having the third height are commonly connected to form the second word line WL**2**. The first conductive materials **241** to **243** having the fourth height are commonly connected to form the third word line WL**3**. The first conductive materials **251** to **253** having the fifth height are commonly connected to form the dummy word line DWL. The first conductive materials **261** to **263** having the sixth height are commonly connected to form the fourth word line WL**4**. The first conductive materials **271** to **273** having the seventh height are commonly connected to form the fifth word line WL**5**. The first conductive materials **281** to **283** having the eighth height are commonly connected to form the sixth word line WL**6**.

The NAND strings NS of the same row share the string select line SSL. The NAND strings NS of different rows are connected to different string select lines SSL**1**, SSL**2** and SSL**3**, respectively. The first to third string select lines SSL**1** to SSL**3** correspond to the first conductive materials **291** to **293** having the ninth height, respectively.

Hereinafter, first string select transistors SST**1** are defined as the string select transistors SST connected to the first string select line SSL**1**. Second string select transistors SST**2** are defined as the string select transistors SST connected to the second string select line SSL**2**. Third string select transistors SST**3** are defined as the string select transistors SST connected to the third string select line SSL**3**.

The common source line CSL is commonly connected to all the NAND strings NS. For example, the first to fourth doping regions **311** to **314** are connected to each other to thereby form the common source line CSL.

As illustrated in FIG. 7, the word lines WL having the same height are commonly connected. Therefore, when the word line WL with a specific height is selected, all of the NAND strings NS connected to the selected word line WL are selected.

The NAND strings of different rows are connected to different string select lines SSL. Accordingly, among the NAND strings NS connected to the same word line WL, the NAND strings NS of the unselected row may be electrically isolated from the corresponding bit line and the NAND strings NS of the selected row may be electrically connected to the corresponding bit line by selecting and unselecting the string select lines SSL**1** to SSL**3**.

That is, by selecting and unselecting the string select lines SSL**1** to SSL**3**, the row of the NAND stings NS may be selected. A column of the NAND strings NS of the selected row may be selected.

Exemplarily, one of the string select lines SSL1 to SSL**3** is selected during program and read operations. That is, the program and read operations are performed in units of rows of the NAND strings NS**11** to NS**13**, NS**21** to NS**23**, and NS**31** to NS**33**.

Exemplarily, a select voltage is applied to the selected word line of the selected row during the program or read operations, and an unselect voltage is applied to the unselected word lines and the dummy word line DWL. For example, the select voltage is a program voltage Vpgm or selection read voltage Vrd. For instance, the unselect voltage is a pass voltage Vpass or non-selection read voltage Vread. That is, the program and read operations are performed in units of word lines of the selected row of the NAND strings NS**11** to NS**13**, NS**21** to NS**23**, and NS**31** to NS**33**.

Exemplarily, among the first conductive materials **211** to **291**, **212** to **292**, and **213** to **293**, the thickness of the insulation material **112** provided between the first conductive material acting as the select lines and the first conductive material acting as the word lines may be greater than the thickness of other insulation materials **112**.

In FIGS. **4** to **7**, the first conductive materials **211**, **212** and **213** having the first height operates as the ground select line GSL, and the first conductive materials **291**, **292** and **293** having the ninth height operates as the string select lines SSL1, SSL**2** and SSL**3**.

Here, the insulation materials **112** provided between the first conductive materials **211**, **212** and **213** having the first height and the first conductive materials **221**, **222** and **223** having the second height may be greater in thickness than the insulation materials **112** provided between the first conductive materials **221**, **222** and **223** having the second height and the conductive materials **281**, **282** and **283** having the eighth height.

Likewise, the insulation materials **112** provided between the first conductive materials **281**, **282** and **283** having the eighth height and the first conductive materials **291**, **292** and **293** having the ninth height may be greater in thickness than the insulation materials **112** provided between the first conductive materials **221**, **222** and **223** having the second height and the conductive materials **281**, **282** and **283** having the eighth height.

FIG. **8** is a circuit diagram illustrating example embodiments in which the memory cells MC of the memory block BLKi_**1** form sub blocks. Referring to FIG. **8**, in the memory block BLKi_**1**, the first to third memory cells MC**1** to MC**3** provided between the dummy memory cells DMC and the ground select transistors GST constitute a first sub block. The fourth to sixth memory cells MC**4** to MC**6** provided between the dummy memory cells DMC and the string select transistors SST constitute a second sub block. In example embodiments, the dummy memory cells DMC act as a separator to separate the first sub block from the second sub block

Exemplarily, an erase operation is performed in units of sub blocks. For example, each sub block is independently erased. For example, the second sub block may be erase-inhibited while the first sub block is being erased. The first sub block may be erase-inhibited while the second sub block is being erased. That is, in each of the NAND strings NS, while some (e.g., MC**1** to MC**3**) of the memory cells MC**1** to MC**6** are being erased, the other memory cells (e.g., MC**4** to MC**6**) may be erase-inhibited.

FIG. **9** is a table illustrating example embodiments of conditions of voltages which are applied to the memory block BLKi_**1** of FIG. **8** during an erase operation. Referring to FIGS. **8** and **9**, the string select lines SSL**1** to SSL**3** are floated. The word lines WL of the unselected sub block are floated. A word line erase voltage Vwe is applied to the word lines WL of the selected sub block. A first dummy word line voltage Vdwl**1** is applied to the dummy word line DWL. The ground select line GSL is floated. Then, an erase voltage Vers is applied to the substrate **111**.

For example, it is assumed that the first sub block is selected. During the erase operation, the word line erase voltage Vwe is applied to the word lines WL**1** to WL**3** of the selected first sub block. During the erase operation, the word lines WL**4** to WL**6** of the unselected second sub block are floated.

FIG. **10** is a timing diagram illustrating voltage variations of the memory block BLKi_**1** according to the voltage conditions of FIG. **9**. FIG. **11** is a cross-sectional view of one of the NAND strings of the memory block BLKi_**1**. Hereinafter, the erase operation of the memory block BLKi_**1** will be described with reference to FIG. **11**. Exemplarily, it is assumed that the first sub block is erased and the second sub block is erase-inhibited.

Referring to FIGS. **8** to **11**, the erase voltage Vers is applied to the substrate **111** at a first timing t**1**. For example, the erase voltage Vers may be a high voltage.

The substrate **111** is doped with the same type substance with the surface layer **114** acting as a body in the second direction. Therefore, the erase voltage Vers is transferred to the surface layer **114** of the NAND string NS.

The first conductive material **211** having the first height acts as the ground select line GSL, and acts as the gate (or control gate) of the ground select transistor GST. The ground select line GSL is floated at the first timing t**1**. The first conductive material **211** is affected by coupling from the surface layer **114**. Accordingly, as the voltage of the surface layer **114** increases to the erase voltage Vers, the voltage of the first conductive material **211** acting as the ground select line GSL increases. For example, the voltage of the ground select line GSL rises up to a ground select line voltage Vgsl.

The voltage of the surface layer **114** acting as a body in the second direction is the erase voltage Vers, and the voltage of the first conductive material acting as the gate (or control gate) of the ground select transistor GST is the ground select line voltage Vgsl. Exemplarily, a difference between the erase voltage Vers and the ground select line voltage Vgsl is not so large to induce Fowler-Nordheim tunneling. Therefore, the ground select transistor GST is erase-inhibited.

The first conductive materials **221** to **241** having the second to fourth heights act as the first to third word lines WL**1** to WL**3**, respectively, and act as the gates (or control gates) of the first to third memory cells MC**1** to MC**3**. At the first timing t**1**, the word line erase voltage Vwe is applied to the selected word lines. Accordingly, the word line erase voltage Vwe is applied to the first to third word line voltages WL1 to WL3. For example, the word line voltage Vwe is a low voltage. For example, the word line erase voltage Vwe is a ground voltage.

The voltage of the surface layer **114** acting as the body in the second direction is the erase voltage Vers, and the voltage of the first conductive materials **221** to **241** acting as the gates (or control gates) of the first to third memory cells MC1 to MC3 is the word line erase voltage Vwe. For example, a difference between the erase voltage Vers and the word line erase voltage Vwe induces Fowler-Nordheim tunneling. For example, voltage levels of the erase voltage Vers and the word line erase voltage Vwe may be set so as to induce Fowler-Nordheim tunneling. Therefore, the first to third memory cells MC1 to MC3 of the selected first sub block are erased.

The first conductive materials **261** to **281** having the sixth to eighth heights act as the fourth to sixth word lines WL4 to WL6, and act as gates (or control gates) of the fourth to sixth memory cells MC4 to MC6. The unselected word lines are floated at the first timing t1. The first conductive materials **261** to **281** are affected by coupling from the surface layer **114**. Accordingly, as the voltage of the surface layer **114** increases to the erase voltage Vers, the voltages of the first conductive materials **261** to **281** acting as the fourth to sixth word lines WL4 to WL6 increase. For example, the voltages of the fourth to sixth word lines WL4 to WL6 rises up to an unselected word line voltage Vuwl.

The voltage of the surface layer **114** acting as a body in the second direction is the erase voltage Vers, and the voltages of the first conductive materials **261** to **281** acting as the gates (or control gates) of the fourth to sixth memory cells MC4 to MC6 are the unselected word line voltage Vuwl. Exemplarily, a difference between the erase voltage Vers and the unselected word line voltage Vuwl is not so large to induce Fowler-Nordheim tunneling. Therefore, the fourth to sixth memory cells MC4 to MC6 of the unselected second sub block are erase-inhibited.

The first conductive material **291** having the ninth height acts as the string select line SSL, and acts as the gate (or control gate) of the string select transistor SST. The string select line SSL is floated at the first timing t1. The first conductive material **291** is affected by coupling from the surface layer **114**. Accordingly, as the voltage of the surface layer **114** increases to the erase voltage Vers, the voltage of the first conductive materials **291** acting as the string select line SSL increases. For example, the voltages of the string select line SSL rises up to a string select line voltage Vssl.

The voltage of the surface layer **114** acting as a body in the second direction is the erase voltage Vers, and the voltage of the first conductive material **291** acting as the gate (or control gate) of the string select transistor SST is the string select line voltage Vssl. Exemplarily, a difference between the erase voltage Vers and the string select line voltage Vssl is not so large to induce Fowler-Nordheim tunneling. Therefore, the string select transistor SST is erase-inhibited.

The first conductive material **251** having the fifth height acts as the dummy word line DWL, and acts as the gate (or control gate) of the dummy memory cell DMC. A first dummy word line voltage Vdwl1 is applied to the dummy word line DWL at the first timing t1. Exemplarily, the voltage level of the first dummy word line voltage Vdwl1 is set so as not to induce Fowler-Nordheim tunneling due to a voltage difference between the surface layer **141** and the gate (or control gate) of the dummy memory cell DMC. That is, the dummy memory cell DMC is erase-inhibited.

When the word line erase voltage Vwe is applied to the word lines (e.g., WL1 to WL3) of the selected sub block, voltages of the word lines (e.g., WL4 to WL6) of the unselected sub block rise up to the unselected word line voltage Vuwl due to coupling. At this time, the word lines WL4 to WL6 of the unselected sub block may be affected by coupling from the word line erase voltage Vwe applied to the word lines WL1 to WL3 of the selected sub block. That is, owing to the coupling effect from the word lines WL1 to WL3 of the selected sub block, a voltage increment of the word lines WL4 to WL6 of the unselected sub block may be decreased.

Likewise, the word lines WL1 to WL3 of the selected sub block may be affected by coupling from the word lines WL4 to WL6 of the unselected sub block. That is, the voltages of the word lines WL1 to WL3 of the selected sub block may be increased due to the coupling effect from the word lines WL4 to WL6 of the unselected sub block.

The dummy word line DWL is provided between the first and second sub blocks. Exemplarily, the first dummy word line voltage Vdwl1 is set to have a voltage level between the word line erase voltage Vwe and the erase voltage Vers. More specifically, the first dummy word line voltage Vdwl1 is set to have a voltage level between the word line erase voltage Vwe and the unselected word line voltage Vuwl. The electric field between the word lines WL1 to WL3 of the selected sub block and the word lines WL4 to WL6 of the unselected sub block is relieved by the first dummy word line voltage Vdwl1 of the dummy word line DWL.

Therefore, a decrease in voltage increment of the word lines WL4 to WL6 of the unselected sub block is prevented by virtue of coupling from the word lines WL1 to WL3 of the selected sub block. Furthermore, an increase in voltages of the word lines WL1 to WL3 of the selected sub block is prevented by virtue of coupling from the word lines WL4 to WL6 of the unselected sub block. Also, the electric field between the word lines WL1 to WL3 of the selected sub block and the word lines WL4 to WL6 of the unselected sub block prevents hot carriers from being generated.

In example embodiments above, it has been described that the word line erase voltage Vwe and the first dummy word line voltage Vdwl1 are applied at the first timing. However, the erase voltage Vers, the word line erase voltage Vwe, and the first dummy word line voltage Vdwl1 may be applied in sequence according to a preset order. For example, at least one voltage of the erase voltage Vers, the word line erase voltage Vwe, and the first dummy word line voltage Vdwl1 may be applied prior to or after other at least one voltage of the erase voltage Vers, the word line erase voltage Vwe, and the first dummy word line voltage Vdwl1. In another example, two voltages of the erase voltage Vers, the word line erase voltage Vwe, and the first dummy word line voltage Vdwl1 may be applied prior to or after another voltage of the erase voltage Vers, the word line erase voltage Vwe, and the first dummy word line voltage Vdwl1.

FIG. **12** is a graph illustrating threshold voltages of the memory cells MC which are measured while varying the first dummy word line voltage Vdwl1. In FIG. **12**, the horizontal axis represents the number of erase cycles, and the vertical axis represents threshold voltages of the memory cells MC.

Exemplarily, it is assumed that the erase operation is performed on the first sub block. The threshold voltages shown in FIG. **12** represent threshold voltage variations of the memory cells of the selected first sub block.

First and second threshold voltage lines Vth1 and Vth2 represent variations of the threshold voltages of the memory cells MC according to the number of erase cycles when the first dummy word line voltage Vdwl1 is set to 12 V. For example, the first threshold voltage line Vth1 represents threshold voltage variations of the dummy memory cell DMC and the memory cell MC3 adjacent thereto. The second threshold voltage line Vth2 represents the memory cells MC1 and MC2 in the first sub block.

Third and fourth threshold voltage lines Vth3 and Vth4 represent variations of the threshold voltages of the memory cells MC according to the number of erase cycles when the first dummy word line voltage Vdwl1 is set to 8 V. For example, the third threshold voltage line Vth3 represents threshold voltage variations of the dummy memory cell DMC and the memory cell MC3 adjacent thereto. The fourth threshold voltage line Vth4 represents the memory cells MC1 and MC2 in the first sub block.

When the first dummy word line voltage Vdwl1 is set to 12 V, a difference between the threshold voltage of the memory cell MC3 adjacent to the dummy word line DWL and the threshold voltages of the memory cells MC1 and MC2 in the first sub block increases as the number of erase cycles of the first sub block increases. That is, as the number of erase cycles of the first sub block increases, a threshold voltage distribution of the memory cells MC1 to MC3 in an erase state increases.

When the first dummy word line voltage Vdwl1 is set to 8 V, a difference between the threshold voltage of the memory cell MC3 adjacent to the dummy word line DWL and the threshold voltages of the memory cells MC1 and MC2 in the sub block is maintained to a reference value or less even though the number of erase cycles of the first sub block increases. That is, even if the number of erase cycles of the first sub block increases, the threshold voltage distribution of the memory cells MC1 to MC3 in the erase state is maintained.

FIG. 13 is a table illustrating example embodiments of conditions of voltages which are applied to the memory block BLKi_1 of FIG. 8 during an erase operation. Referring to FIGS. 8 and 13, the string select lines SSL1 to SSL3 are floated during the erase operation. The word line erase-inhibit voltage Vwei is applied to the word lines WL of the unselected sub block. The word line erase voltage Vwe is applied to the word lines WL of the selected sub block. The second dummy word line voltage Vdwl2 is applied to the dummy word line DWL. The ground select line GSL is floated. The erase voltage Vers is applied to the substrate 111.

Exemplarily, it is assumed that the first sub block is selected. During the erase operation, the word line erase voltage Vwe is applied to the word lines WL1 to WL3 of the selected first sub block. During the erase operation, the word line erase-inhibit voltage Vwei is applied to the word lines WL4 to WL6 of the unselected second sub block.

FIG. 14 is a timing diagram illustrating voltage variations of the memory block BLKi_1 according to the voltage conditions of FIG. 13. FIG. 15 is a cross-sectional view of one of the NAND strings of the memory block BLKi_1. Hereinafter, the erase operation of the memory block BLKi_1 will be described with reference to FIG. 14. Exemplarily, it is assumed that the first sub block is erased and the second sub block is erase-inhibited.

Voltage conditions and voltage variations of FIG. 14 are identical to those described in FIGS. 9 to 11, except that the word line erase-inhibit voltage Vwei is applied to the word lines WL4 to WL6 of the unselected sub block and the second dummy word line voltage Vdwl2 is applied to the dummy word line DWL. Therefore, duplicate description will be omitted herein.

Referring to FIGS. 13 to 15, the erase voltage Vers is applied to the substrate 111 at the first timing t1. Exemplarily, the erase voltage Vers may be a high voltage.

The substrate 111 is doped with the same type substance with the surface layer 114 acting as a body in the second direction. Therefore, the erase voltage Vers is transferred to the surface layer 114 of the NAND string NS.

The first conductive materials 261 to 281 having the sixth to eighth heights act as the fourth to sixth word lines WL4 to WL6, respectively, and act as the gates (or control gates) of the fourth to sixth memory cells MC4 to MC6. At the first timing t1, the word line erase-inhibit voltage Vwei is applied to the unselected word lines.

The voltage of the surface layer 114 acting as the body in the second direction is the erase voltage Vers, and the voltage of the first conductive materials 261 to 281 acting as the gates (or control gates) of the fourth to sixth memory cells MC4 to MC6 is the word line erase voltage Vwe. For example, a voltage level of the word line erase-inhibit voltage Vwei may be set so as not to induce Fowler-Nordheim tunneling due to a voltage difference between the word line erase-inhibit voltage Vwei and the erase voltage Vers. For example, the word line erase-inhibit voltage Vwei may be a high voltage. Therefore, the fourth to sixth memory cells MC4 to MC6 of the selected second sub block are erase-inhibited.

The first conductive material 251 having the fifth height acts as the dummy word line DWL, and acts as the gate (or control gate) of the dummy memory cell DMC. A second dummy word line voltage Vdwl2 is applied to the dummy word line DWL at the first timing t1. Exemplarily, the voltage level of the second dummy word line voltage Vdwl2 is set so as not to induce Fowler-Nordheim tunneling due to a voltage difference between the surface layer 141 and the gate (or control gate) of the dummy memory cell DMC. That is, the dummy memory cell DMC is erase-inhibited.

The dummy word line DWL is provided between the first and second sub blocks. Exemplarily, the second dummy word line voltage Vdwl2 is set to have a voltage level between the word line erase voltage Vwe and the word line erase-inhibit voltage Vwei. The electric field between the word lines WL1 to WL3 of the selected sub block and the word lines WL4 to WL6 of the unselected sub block is relieved by the first dummy word line voltage Vdw1 of the dummy word line DWL.

Therefore, a decrease in voltage increment of the word lines WL4 to WL6 of the unselected sub block is prevented by virtue of coupling from the word lines WL1 to WL3 of the selected sub block. Furthermore, an increase in voltages of the word lines WL1 to WL3 of the selected sub block is prevented by virtue of coupling from the word lines WL4 to WL6 of the unselected sub block. Also, the electric field between the word lines WL1 to WL3 of the selected sub block and the word lines WL4 to WL6 of the unselected sub block prevents hot carriers from being generated.

In the example embodiments above, it has been described that the erase voltage Vers, the word line erase voltage Vwe, the word line erase-inhibit voltage Vwei, and the second dummy word line voltage Vdwl2 are applied at the first timing. However, the erase voltage Vers, the word line erase voltage Vwe, the word line erase-inhibit voltage Vwei, and the second dummy word line voltage Vdwl2 may be applied in sequence according to a preset order.

As described above, in the nonvolatile memory device 100 (see FIGS. 1 and 2) according to example embodiments of inventive concepts, the erase operation is performed in unit of sub blocks. That is, the erase operating unit is reduced to sub blocks from memory blocks BLK. When the erase operating unit is reduced, a time required for a background operation such as merge, garbage collection, refresh operations is reduced. Accordingly, the operating speed of the nonvolatile memory device 100 may be improved. Also, the operating speed of the memory system **1000** including the nonvolatile memory device **100** may be improved.

As described above, a dummy memory cell DMC is provided between sub blocks. Exemplarily, the first dummy word line voltage Vdwl**1** having a voltage level between the word line erase voltage Vwe and the unselected word line voltage Vuwl is applied is applied to the dummy memory cell DMC during the erase operation. As another example, the second dummy word line voltage Vdwl**2** having a voltage level between the word line erase voltage Vwe and the word line erase-inhibit voltage Vwei is applied to the dummy memory cell DMC during the erase operation. Therefore, the reliability of the nonvolatile memory device **100** and the reliability of the memory system **1000** including the same may be improved because the electric field between the sub blocks is relieved.

FIG. **16** is a diagram illustrating example embodiments of the threshold voltage distribution of the memory cells MC of the memory block BLKi_**1** in FIG. **8**. In FIG. **16**, a horizontal axis represents threshold voltages of the memory cells MC, and a vertical axis represents the number of memory cells. Exemplarily, FIG. **16** illustrates the threshold voltage distribution of the memory cells MC in which one bit is stored in each cell. Referring to FIGS. **8** and **16**, the memory cells MC have one of an erase state E and a program state P.

During a read operation, a select read voltage Vr is applied to the selected word line. The select read voltage Vr has a voltage level between the threshold voltages of the memory cells in the erase state E and the threshold voltages of the memory cells in the program state P. That is, among the memory cells MC connected to the selected word line, the memory cells of the erase state E are turned off, and the memory cells of the program state P are turned on.

During the read operation, a first unselect read voltage Vread**1** is applied to the unselected word lines. The first unselect read voltage Vread**1** has a high voltage level than the threshold voltages of the memory cells MC. For example, the first unselect read voltage Vread**1** may be a high voltage. That is, the memory cells MC connected to the unselected word line are turned on.

During the read operation, a turn-on voltage is applied to the dummy word line. The turn-on voltage is a voltage turning on the dummy cells DMC. For example, the turn-on voltage may be a first unselect read voltage Vread**1**.

FIG. **17** is a diagram illustrating example embodiments of the threshold voltage distribution of the memory cells MC of the memory block BLKi_**1** in FIG. **8**. In FIG. **16**, a horizontal axis represents threshold voltages of the memory cells MC, and a vertical axis represents the number of memory cells. Exemplarily, FIG. **16** illustrates the threshold voltage distribution of the memory cells MC in which one bit is stored in each cell. Referring to FIGS. **8** and **16**, the memory cells MC have one of an erase state E and a program state P.

During the read operation, at least two of first to third select read voltages Vr**1** to Vr**3** are sequentially applied to the selected word line. Whenever one of the first to third select read voltages Vr**1** to Vr**3** is applied to the selected word line, the second unselect read voltage Vread**2** is applied to the unselected word line and the turn-on voltage is applied to the dummy word line DWL. For example, the turn-on voltage may be the second unselect read voltage Vread**2**.

Like the description with reference to FIGS. **16** and **17**, the first unselect read voltage Vread**1** or the second unselect read voltage Vread**2** is applied to the unselected word lines during the read operation. The first and second unselected read voltages Vread**1** and Vread**2** have voltage levels higher than the threshold voltages of the memory cells MC. For example, the first and second unselect read voltages Vread**1** and Vread**2** may be a high voltage.

During the read operation, the threshold voltages of the memory cells MC connected to the unselected word lines may vary due to the first unselect read voltage Vread**1** or second unselect read voltage Vread**2**. For example, the threshold voltages of the memory cells MC connected to the unselected word lines may be increased. That is, a read disturb may occur. When the read disturb occurs, data stored in the memory cells MC may be lost.

As the number of bits stored in one memory cell increases, the threshold voltage of the memory cell also increases. That is, as the number of bits stored in one memory cell increases, the unselect read voltage also increases. Accordingly, as the number of bits stored in one memory cell increases, the read disturb becomes more serious.

As illustrated in FIG. **8**, the first and second sub blocks share the NAND strings NS**11** to NS**13**, NS**21** to NS**23**, and NS**31** to NS**33**. More specifically, some of the memory cells MC of each NAND string NS is assigned to the first sub block, and the others are assigned to the second block.

When the read operation is performed in the first sub block, the select read voltage Vr, Vr**1**, Vr**2** or Vr**3** is applied to the selected word line of the first sub block, and the unselect read voltage Vread**1** or Vread**2** is applied to the unselected word lines. The unselect read voltage Vread**1** or Vread**2** is applied to the word lines of the second sub block.

Likewise, when the read operation is performed in the second sub block, the select read voltage Vr, Vr**1**, Vr**2** or Vr**3** is applied to the selected word line of the second sub block, and the unselect read voltage Vread**1** or Vread**2** is applied to the unselected word lines. The unselect read voltage Vread**1** or Vread**2** is applied to the word lines of the first sub block.

That is, when the read operation is performed in one of the sub blocks of the memory block BLKi_**1**, the read disturb may occur in all sub blocks of the memory block BLKi_**1** as well as the sub block where the read operation is being performed.

To solve the above-described problem, the memory system **1000** (see FIG. **1**) according to example embodiments of inventive concepts is configured to refresh the specific sub block of the memory block BLKi_**1** based on the read operation performed in the sub block of the memory block BLKi_**1**.

FIG. **18** is a flowchart illustrating a refresh method according to example embodiments of inventive concepts. Referring to FIGS. **1**, **8**, and **18**, in operation S**110**, data are read from one of the sub blocks of the memory block. For example, data are read from one of the first and second sub blocks.

Exemplarily, data are read in response to a read request from the host. For example, between the first and second sub blocks of the selected memory block BLKi_**1** of the nonvolatile memory device, the controller **500** reads data from the sub block corresponding to a read request from the host.

Exemplarily, the controller **500** reads data from one of the first and second sub blocks of the selected memory block BLKi_**1** of the nonvolatile memory device, which corresponds to a read request from the host according to a predetermined or desired operation schedule. For example, the controller **500** reads data from one of the first and second sub blocks of the selected memory block BLKi_**1** of the nonvolatile memory device **100** during a background operation such as merge, garbage collection, and refresh operations.

In operation S**120**, each sub block of the memory block is selectively refreshed in response to the read operation. For example, in response to the read operation performed in operation S**120**, each sub block of the selected memory block BLKi_**1** is selectively refreshed.

That is, when data are read from one of the sub blocks of the selected memory block BLKi_**1**, it is determined whether each sub block of the selected memory block BLKi_**1** is refreshed. Among the sub blocks of the selected memory block BLKi_**1**, the sub block where read disturb reaches to a reference value is refreshed. For example, whether refresh is performed or not is determined on the basis of the number of read cycles. That is, the sub block where the number of read cycles reaches to a reference value is refreshed among the sub blocks of the selected memory block BLKi_**1**.

The refresh includes an operation of backing up data stored in the specific sub block. For example, the refresh may include reading data stored in the specific sub block, and writing the read data to a sub block of the same memory block BLKi_**1** or another memory block. Exemplarily, the refresh may further include erasing or invalidating the specific sub block in which backup data are stored.

FIG. **19** is a block diagram illustrating a flash translation layer **600** driven in the controller of FIG. **1**. Exemplarily, the flash translation layer **600** is driven by a processor **520** of the controller **500**.

Exemplarily, the flash translation layer **600** is stored in the nonvolatile memory device **100**. In a power-on state, the controller **500** reads the flash translation layer **600** from the nonvolatile memory device **100**. The read flash translation layer **600** is driven by the processor **520**.

Exemplarily, the flash translation layer **600** may be stored in the controller **500**. For example, the controller **500** may further include a nonvolatile memory (not shown) storing the flash translation layer **600**.

Referring to FIGS. **1** and **18**, the flash translation layer **600** performs an interfacing operation between the host and the nonvolatile memory device **100**. For example, the flash translation layer **600** translates a logical block address (LBA) received from the host into a physical block address (PBA) used in the nonvolatile memory device **100**.

The flash translation layer **600** performs background operations of the nonvolatile memory device **100**. For example, the flash translation layer **600** may perform operations such as merge, garbage collection, wear-leveling, and refresh.

The flash translation layer **600** includes a mapping table **610**, a read cycle table **620**, and/or a refresh unit **630**. The mapping table **610** is configured to store mapping information between LBA and PBA.

The read cycle table **620** is configured to store the number of read cycles of each sub block of the memory blocks BLK**1** to BLKz of the nonvolatile memory device **100**.

The refresh unit **630** is configured to selectively refresh each sub block of the nonvolatile memory device **100** based on the number of read cycles of each sub block stored in the read cycle table **620**.

FIG. **20** is a flow chart illustrating a method of operating the refresh unit **630** of FIG. **19**. Exemplarily, the number of read cycles of the first and second sub blocks of the selected memory block BLKi_**1** is assumed to have values in Table 1 below.

TABLE 1

Sub block	Number of read cycles
First sub block	a
Second sub block	b

Referring to FIGS. **19** and **20**, in operation S**210**, reading is detected from one of the sub blocks of the selected memory block BLKi_**1**. For example, when reading is performed in the selected sub block of the selected memory block BLKi_**1**, the refresh unit **630** is called. That is, since the refresh unit **630** is activated when reading is performed in the selected sub block, it may be understood that the refresh unit **630** is activated when reading is detected from the selected sub block. Exemplarily, when reading is performed in the selected sub block, an address of the selected sub block is transferred to the refresh unit **630**.

In operation S**220**, the number of read cycles of the sub blocks of the selected memory block BLKi_**1** is counted up. When data is read in the first or second sub block of the selected memory block BLKi_**1**, the refresh unit **630** counts up the numbers of read cycles of both of the first and second sub blocks. Here, the number of read cycles of the sub blocks of the selected memory block BLKi_**1** stored in the read cycle table **620** is listed in Table 2 below.

TABLE 2

Sub block	Number of read cycles
First sub block	a + 1
Second sub block	b + 1

In operation S**230**, it is determined whether there exists a sub block having the number of read cycles that reaches to a reference value. For example, the refresh unit **630** determines whether there exists a sub block having the number of read cycles that reaches to the reference value among the sub blocks of the selected memory block BLKi_**1**. If there is no sub block having the number of read cycles that reaches to the reference value, the refresh unit **630** stops operating. If there is a sub block having the number of read cycles that reaches to the reference value, operation S**240** is performed.

In operation S**240**, the sub block having the number of read cycles that reaches to the reference value is refreshed. For example, the refresh unit **630** refreshes the sub block having the number of read cycles that reaches to the reference value. If there are two or more sub blocks having the number of read cycles that reaches to the reference value in the selected memory block BLKi_**1**, the refresh unit **630** refreshes at least two sub blocks having the number of read cycles that reaches to the reference value.

Exemplarily, data are read from the sub block to be refreshed under control of the refresh unit **630**. The read data are stored in the RAM **530**. Thereafter, under control of the refresh unit **630**, data stored in the RAM **530** are written to a free sub block of the nonvolatile memory device **100**. For example, the read data are written to a free sub block of the selected memory block BLKi_**1** or a free sub block of a memory block other than the selected memory block BLKi_**1**.

Exemplarily, a refresh may be performed in the nonvolatile memory device **100** under control of the refresh unit **630**. Under control of the refresh unit **630**, the read & write circuit **130** (see FIG. **2**) reads data of which volume corresponds to a read unit from the sub block to be refreshed. Thereafter, the read & write circuit **130** writes the read data to the free sub block. The read & write circuit **130** repeats read/write operation until all data of the sub block to be refreshed are written to the free sub block. That is, refresh may be performed based on a copy-back operation.

Exemplarily, when a read cycle of a specific sub block of the selected memory block BLKi_**1** reaches to the reference value after the reading of the selected sub block of the selected memory block **BLKi_1**, the refresh unit **630** may refresh the specific sub block following the reading of the selected sub block.

Exemplarily, when a read cycle of a specific sub block of the selected memory block **BLKi_1** reaches to the reference value after the reading of the selected sub block of the selected memory block **BLKi_1**, the refresh unit **630** makes a reservation for refreshing of the specific sub block. When the memory system **100** is in an idle state, the refresh unit **630** may perform refresh operation on the specific sub block. In the case where the read operation upon the sub block of the memory block **BLKi_1** corresponding to the specific sub block is requested in a state that the refresh of the specific sub block is reserved, the refresh unit **630** may refresh the specific sub block before the read operation is performed.

In operation S**250**, the number of read cycles of the refreshed sub block is reset. Exemplarily, it is assumed that the first sub block of the selected memory block **BLKi_1** is reset. Here, the number of read cycles of the sub blocks of the selected memory block **BLKi_1** stored in the read cycle table **620** is listed in Table 3 below.

TABLE 3

Sub block	Number of read cycles
First sub block	0
Second sub block	b + 1

Exemplarily, after the first sub block is refreshed, the first sub block may be invalidated. For example, in the mapping table **610**, the first sub block may be set as an invalidation data block.

Exemplarily, the first sub block may be erased after the first sub block is refreshed. For example, in succession to the refresh of the first sub block, the first sub block may be erased.

Exemplarily, an erase operation of the first sub block may be reserved after the first sub block is refreshed. For example, when the memory system **1000** is in an idle state, the first sub block may be erased.

In summary, when the read operation is performed in the selected sub block of the sub blocks of the memory block **BLKi_1**, each sub block of the memory block **BLKi_1** is selectively refreshed. For example, when data is written to a specific sub block of the memory block **BLKi_1**, and thereafter the number of read cycles performed in the sub blocks of the memory block **BLKi_1** reaches to the reference value, the specific sub block is refreshed. Since a read disturb caused by the read operation of the sub blocks of the memory block **BLKi_1** is compensated, the reliability of the nonvolatile memory device **100** and the reliability of the memory system **1000** including the same may be improved.

In the foregoing example embodiments, it has been described that 1 bit or 2 bits is(are) stored in each memory cell MC. However, it is not limited that each memory cell MC store 1 bit or 2 bits. Each of the memory cells MC may store at least 3 bits.

In the foregoing example embodiments, it has been described that the memory block **BLKi_1** includes the first and second sub blocks. However, it is not limited that the memory block **BLKi_1** includes two sub blocks. For example, the memory block **BLKi_1** may include three or more sub blocks. When a plurality of sub blocks are provided, the memory block **BLKi_1** includes at least one dummy word line DWL and the dummy memory cell DMC disposed between the sub blocks.

FIG. **21** is a block diagram schematically illustrating a flash translation layer driven by a controller in FIG. **1** according to example embodiments of inventive concepts. Referring to FIG. **21**, a flash translation layer **600***a* includes a mapping table **610**, a disturb count table **620***a*, and a refresh/reclaim unit **630***a*.

The mapping table **610** maps logical addresses and physical addresses.

The disturb count table **620***a* counts disturb influence (e.g., disturb-generated number) by the memory block or by the sub block.

As described in relation to FIGS. **16** and **17**, upon a read operation on a memory block including a plurality of sub blocks, read disturb arises from all sub blocks. The disturb of the memory block including a plurality of sub blocks is generated not only at a read operation but also at program and erase operations.

When a program operation is executed, a program voltage is supplied to a selected word line, and a pass voltage is supplied to unselected word lines. The pass voltage is provided to word lines of unselected sub blocks of the memory block. The pass voltage may be a high voltage enough to turn on all memory cells regardless of threshold voltages of the memory cells. The program voltage may be a high voltage enough to generate the Fowler-Nordheim tunneling. That is, when the program operation is performed, program disturb is generated at unselected sub blocks due to the pass voltage. Further, program disturb is generated at a selected sub block due to the pass voltage and the program voltage.

Upon program verification, a verification voltage is supplied to a selected word line, and a non-selection read voltage Vread is provided to unselected word lines. That is, when a program verification operation is performed, the unselected sub block and the selected sub block experience disturb due to the non-selection read voltage Vread.

When an erase operation is performed, an erase voltage Vers is supplied to a surface layer **114** of sub blocks. When the erase voltage is supplied to the surface layer **114**, word lines are provided with a ground voltage VSS, and then the word lines are floated. In case that the ground voltage VSS is supplied to the word lines, the memory cells are disturbed due to the erase voltage Vers.

When an erase verification operation is performed, an erase verification voltage is supplied to word lines of a selected sub block, and a non-selection read voltage Vread is supplied to word lines of unselected sub blocks. Thus, disturb is generated at the unselected sub blocks due to the non-selection read voltage Vread.

As described above, the disturb of a memory block including a plurality of sub blocks is generated not only at a read operation but also at program and erase operations. The disturb count table **620***a* counts disturb influence (e.g., disturb-generated number) by the memory block or by the sub block when programming, reading, and erasing are performed at a memory block.

The refresh/reclaim unit **630***a* generate a command referring to the disturb count table **620***a* so as to perform a refresh or reclaim operation. The refresh operation may be an operation where data of a first memory block (or, a first sub block) is copied to a second memory block (or, a second sub block). The reclaim operation may include reading a memory block (or, a sub block), erasing the memory block (or, the sub block), and rewriting the read data in a memory block (or, a sub block). The refresh and reclaim operations may be an operation of improving the reliability of data by reprogramming data the stability of which is lowered as a disturb count reaches a reference value.

FIG. **22** is a flowchart illustrating a control method of controlling a nonvolatile memory device via a flash translation layer in FIG. **21**. Referring to FIGS. **21** and **22**, in operation S**310**, a flash translation layer **600***a* compares a count value of a memory block (or, a sub block of the memory block) with a reference value. Herein, the count value of the memory block may be determined according to the number of program, read, and erase operations executed at the memory block (or, a sub block of the memory block) after data is programmed in the memory block (or, the sub block of the memory block) of a nonvolatile memory device **100**. A refresh/reclaim unit **630***a* detects the count value of the memory block (or, the sub block of the memory block) referring to a disturb count table **620***a*.

In operation S**320**, the flash translation layer **600***a* performs refreshing or reclaiming when the count value is identical to or larger than the reference value.

FIG. **23** is a flowchart for describing a control method of FIG. **22** according to example embodiments of inventive concepts. Referring to FIGS. **1** and **21** to **23**, in operation S**410**, there is generated a program, read, or erase command of one sub block of sub blocks of a first memory block. A flash translation layer **600***a* may generate the program, read, or erase command according to a command from an external host, according to desired (or alternatively predetermined scheduling), or as occasion needs.

In operation S**420**, there is transmitted a program, read, or erase command of a sub block of the first memory block. The flash translation layer **600***a* sends the generated program, read, or erase command to a nonvolatile memory device **100**. The nonvolatile memory device **100** performs a program, read, or erase operation on the sub block of the first memory block in response to the program, read, or erase command.

In operation S**430**, there is judged whether a count value of the first memory block is equal to or larger than a reference value TV. A refresh/reclaim unit **630***a* of the flash translation layer **600***a* detects a count value of the first memory block referring to a disturb count table **620***a*, and may compare the detected count value with the reference value TV. The reference value TV may be maximum disturb (or, the number of maximum disturb) where the integrity of data programmed in memory cells is secured. The reference value TV may be determined according to a physical characteristic of the nonvolatile memory device **100**. The reference value TV may be judged by a maker of the nonvolatile memory device **1000**, and may be stored in the nonvolatile memory device **100**. The flash translation layer **600***a* may use the reference value TV stored in the nonvolatile memory device **100**.

If the count value of the first memory block is equal to or larger than the reference value TV, in operation S**440**, a command for refreshing to a second memory block from a first memory block is transferred. The flash translation layer **600***a* may send a refresh command to the nonvolatile memory device **100**. In response to the refresh command, the nonvolatile memory device **100** performs a refresh operation. The nonvolatile memory device **100** reads data from the first memory block, and may reprogram the second memory block with the read data.

In operation S**450**, a count value of the second memory block is increased due to the refresh operation. Upon refreshing, a program operation is performed at the second memory block. That is, when a refresh operation is executed, a count value of the second memory block may be increased. The flash translation layer **600***a* may increase a count value of the second memory block stored in the disturb count table **620***a* according to disturb of the second memory block generated at the refresh operation.

In operation S**460**, the first memory block is invalidated. The flash translation layer **600***a* treats the first memory block to be a dirty memory block. The flash translation layer **600***a* may erase the first memory block at an idle time.

If a count value of the first memory block is smaller than the reference value TV, in operation S**470**, a count value of the first memory block is increased according programming, reading, or erasing. The flash translation layer **600***a* judges disturb due to programming, erasing, or reading executed according to a command transferred in operation S**420**, and may increase a count value of the first memory block according to a judgment result.

In example embodiments, when the first memory block (or, the second memory block) is erased, a count of the first memory block (or, the second memory block) is reset.

In example embodiments, after data is programmed in at least one memory cell of the first memory block (or, the second memory block), a count value of the first memory block (or, the second memory block) is increased according to programming, reading, or erasing executed at the first memory block (or, the second memory block). Alternatively, after data is programmed in memory cells of the first memory block (or, the second memory block), a count value of the first memory block (or, the second memory block) is increased according to programming, reading, or erasing executed at the first memory block (or, the second memory block). In this case, there is skipped an operation S**450** of increasing a count value of the second memory block according to a refresh operation.

FIGS. **24** and **25** are flowcharts for describing a control method of FIG. **22** according to example embodiments of inventive concepts. Referring to FIGS. **1**, **21**, and **24**, in operation S**510**, there is generated a program, read, or erase command of one sub block of sub blocks of a first memory block.

In operation S**520**, there is judged whether a count value of the first memory block is equal to or larger than a reference value TV. If the count value of the first memory block is equal to or larger than the reference value TV, in operation S**530**, a command for refreshing to a second memory block from a first memory block is transferred. The flash translation layer **600***a* may send a refresh command to the nonvolatile memory device **100**. In response to the refresh command, the nonvolatile memory device **100** performs a refresh operation. The nonvolatile memory device **100** reads data from the first memory block, and may reprogram the second memory block with the read data.

In operation S**540**, the flash translation layer **600***a* sends a program or read command of a sub block of sub blocks of a second memory block. The sub block of the second memory block may be a sub block in which data of the sub block of the first memory block is reprogrammed. In response to the program or read command, the nonvolatile memory device **100** performs reading or programming on the sub block of the second memory block.

In operation S**550**, the flash translation layer **600***a* increases a count value of the second memory block according to refreshing and programming or reading. Refreshing is made at the second memory block, and then reading or programming is performed. Thus, the second memory block suffers from disturb due to refreshing and programming or reading. The flash translation layer **600***a* increases a count value of the second memory block according to refreshing and programming or reading.

In operation S**560**, the flash translation layer **600***a* invalidates the first memory block.

If a count value of the first memory block is smaller than the reference value TV, in operation S**570**, a program or read command on the sub block of the first memory block is sent. The flash translation layer **600***a* may send a program or read command to the nonvolatile memory device **100**. In response to the program or read command, the nonvolatile memory device **100** performs reading or programming on the sub block of the first memory block.

In operation S**580**, the flash translation layer **600***a* increases a count value of the first memory block according to programming or reading.

Referring to FIGS. **1**, **21**, and **25**, in operation S**610**, an erase command on one sub block of sub blocks of the first memory block is generated.

In operation S**620**, the flash translation layer **600***a* judges whether a count value of the first memory block is equal to or larger than the reference value TV.

If a count value of the first memory block is equal to or larger than the reference value TV, in operation S**630**, the flash translation layer **600***a* sends a command for refreshing from the first memory block to the second memory block except for one sub block corresponding to an erase command. In response to the refresh command, the nonvolatile memory device **100** reads data of the first memory block other than one sub block to reprogram the read data in the second memory block.

In operation S**640**, the flash translation layer **600***a* increases a count value of the second memory block according to refreshing. In operation S**650**, the flash translation layer **600***a* invalidates the first memory block.

If a count value of the first memory block is smaller than the reference value TV, in operation S**660**, the flash translation layer **600***a* provides the nonvolatile memory device **100** with an erase command associated with one sub block of the first memory block. In response to the erase command, the nonvolatile memory device **100** erases the sub block of the first memory block. In operation S**670**, the flash translation layer **600***a* increases a count value of the first memory block according to erasing.

In example embodiments, when the first memory block (or, the second memory block) is erased, a count of the first memory block (or, the second memory block) is reset.

In example embodiments, after data is programmed in at least one memory cell of the first memory block (or, the second memory block), a count value of the first memory block (or, the second memory block) is increased according to programming, reading, or erasing executed at the first memory block (or, the second memory block). Alternatively, after data is programmed in memory cells of the first memory block (or, the second memory block), a count value of the first memory block (or, the second memory block) is increased according to programming, reading, or erasing executed at the first memory block (or, the second memory block). In this case, there is skipped an operation S**550** of increasing a count value of the second memory block according to a refresh operation and an operation S**640** of increasing a count value of the second memory block.

FIG. **26** is a flowchart for describing a control method of FIG. **22** according to example embodiments of inventive concepts. Referring to FIGS. **1**, **21**, and **26**, in operation S**710**, there is generated a program, read, or erase command of one sub block of sub blocks of a first memory block.

In operation S**720**, a flash translation layer **600***a* sends a program, read, or erase command of one sub block of the first memory block to the nonvolatile memory device **100**. In response to the transferred command, the nonvolatile memory device **100** performs programming, reading, or erasing on one sub block of the first memory block.

In operation S**730**, the flash translation layer **600***a* increases a count value of the first memory block according to programming, reading, or erasing.

In operation S**740**, the flash translation layer **600***a* judges whether a count value of the first memory block is equal to or larger than a reference value TV. If the count value of the first memory block is smaller than the reference value TV, programming, reading, or erasing may be ended.

If the count value of the first memory block is equal to or larger than the reference value TV, in operation S**750**, the flash translation layer **600***a* provides the nonvolatile memory device **100** with a command for refreshing to a second memory block from a first memory block. In response to the refresh command, the nonvolatile memory device **100** reads data from the first memory block, and may reprogram the second memory block with the read data.

In operation S**760**, the flash translation layer **600***a* increases a count value of the second memory block according to refreshing. In operation S**770**, the flash translation layer **600***a* invalidates the first memory block.

In example embodiments, when the first memory block (or, the second memory block) is erased, a count of the first memory block (or, the second memory block) is reset.

In example embodiments, after data is programmed in at least one memory cell of the first memory block (or, the second memory block), a count value of the first memory block (or, the second memory block) is increased according to programming, reading, or erasing executed at the first memory block (or, the second memory block). Alternatively, after data is programmed in memory cells of the first memory block (or, the second memory block), a count value of the first memory block (or, the second memory block) is increased according to programming, reading, or erasing executed at the first memory block (or, the second memory block). In this case, there is skipped an operation S**760** of increasing a count value of the second memory block according to a refresh operation.

As described above, the flash translation layer **600***a* manages a count value indicating disturb influence (e.g., disturb-generated number) by the memory block. If a count value of a specific memory block is equal to or larger than a reference value TV, the flash translation layer **600***a* controls the nonvolatile memory device **100** such that data of the specific memory block is reprogrammed in another memory block. Thus, it is possible to provide a control method of the nonvolatile memory device with improved reliability.

FIG. **27** is a flowchart for describing an operation of increasing a count value of a memory block according to example embodiments of inventive concepts. In FIG. **27**, there is illustrated an example embodiment that a count value of a memory block is increased when a program operation on a memory block is performed.

Referring to FIGS. **21** and **27**, in operation S**810**, a flash translation layer **600***a* receives a program result including the number of program loops from a nonvolatile memory device **100** that performed programming. Each program loop includes applying of program and pass voltages and program verifying. That is, each program loop may cause one disturb due to the program and pass voltages and one disturb due to a non-selection read voltage Vread at program verifying. In case that N program loops are iterated at programming, a programmed memory block may experience the disturb N times due to the program and pass voltages at programming and the disturb N times due to the non-selection read voltage Vread at program verifying.

In operation S820, the flash translation layer **600***a* increases a count value of a memory block according to the number of program loops.

In example embodiments, disturb influence due to programming can be quantitatively decided with an average value via various test operations. The flash translation layer **600***a* increases a count value using the quantitatively decided value instead of the number of program loops.

FIG. **28** is a flowchart for describing an operation of increasing a count value of a memory block according to example embodiments of inventive concepts. In FIG. **28**, there is illustrated an example embodiment that a count value of a memory block is increased when a refresh operation on a memory block is performed.

Referring to FIGS. **21** and **28**, in operation S**830**, a flash translation layer **600***a* receives a refresh result including program and read numbers from a nonvolatile memory device **100**. The refresh operation may accompany a plurality of program operations. In case that the memory block includes Multi-Level Cells, a read operation may be carried out when a bit higher than a Least Significant Bit (LSB) is programmed. That is, the refresh operation may accompany a plurality of program operations and a plurality of read operations. The flash translation layer **600***a* is provided with the numbers of programming and reading executed at the refresh operation from the nonvolatile memory device **100**.

In operation S**840**, the flash translation layer **600***a* increases a count value of a memory block according to the programming and reading numbers. As described in relation to FIG. **27**, the flash translation layer **600***a* may increase a count value using the number of program loops iterated at each program operation and the number of program operations executed.

In example embodiments, disturb influence due to refreshing can be quantitatively decided with an average value via various test operations. The flash translation layer **600***a* increases a count value using the quantitatively decided value instead of the programming and reading numbers.

FIG. **29** is a flowchart for describing an operation of increasing a count value of a memory block according to example embodiments of inventive concepts. In FIG. **29**, there is illustrated an example embodiment that a count value of a memory block is increased when an erase operation on a memory block is performed.

Referring to FIGS. **21** and **29**, in operation S**850**, a flash translation layer **600***a* receives an erase result including the number of erase loops from a nonvolatile memory device **100** that performed programming. Each erase loop includes applying of an erase voltage and erase verifying. That is, each erase loop may cause one disturb due to the erase voltage and one disturb due to a non-selection read voltage Vread at erase verifying. In case that N erase loops are iterated at erasing, an erased memory block may experience the disturb N times due to the erase voltage at erasing and the disturb N times due to the non-selection read voltage Vread at erase verifying.

In operation S**860**, the flash translation layer **600***a* increases a count value of a memory block according to the number of erase loops.

In example embodiments, disturb influence due to erasing can be quantitatively decided with an average value via various test operations. The flash translation layer **600***a* increases a count value using the quantitatively decided value instead of the number of erase loops.

FIG. **30** is a flowchart for describing a control method of FIG. **22** according to example embodiments of inventive concepts. Referring to FIGS. **1**, **21**, and **30**, in operation S**910**, a flash translation layer **600***a* generates a program, read, or erase command associated with one sub block of sub blocks of a first memory block. In operation S**920**, the flash translation layer **600***a* sends the program, read, or erase command associated with one sub block of sub blocks of the first memory block to a nonvolatile memory device **100**. The nonvolatile memory device **100** performs a program, read, or erase operation on the sub block of the first memory block in response to the program, read, or erase command.

In operation S**930**, the flash translation layer **600***a* judges whether a count value of the sub block of the first memory block is equal to or larger than a reference value TV.

If the count value of the sub block of the first memory block is equal to or larger than the reference value TV, in operation S**940**, the flash translation layer **600***a* sends a command for refreshing to a second memory block from a first sub block (a sub block having a count value that reaches the reference value TV) of the first memory block. In response to the refresh command, the nonvolatile memory device **100** reads data from the first sub block of the first memory block, and may reprogram a sub block of the second memory block with the read data.

In operation S**950**, count values of sub blocks of the second memory block are increased according to the refresh operation. When the second memory block experiences a program operation according to the refresh operation, sub blocks of the second memory block may experience program-based disturb. The flash translation layer **600***a* increases count values of sub blocks of the second memory block according to the refresh operation. Count values of sub blocks, having an erase state (i.e., a state where data is not programmed), from among sub blocks of the second memory block are not increased.

In operation S**960**, the flash translation layer **600***a* increases a count value of a second sub block (i.e., a sub block having a count value that does not reach the reference value TV) of the first memory block according to a refresh operation executed at the first memory block and a program, read, or erase operation executed at one sub block of the first memory block. When a program, read, or erase operation is performed on the first sub block of the first memory block, the second sub block of the first memory block may suffer from disturb. When the first sub block is refreshed, the second sub block may experience disturb due to a read operation associated with the refresh operation.

The flash translation layer **600***a* increases a count value of the second sub block of the first memory block according to the refresh operation. For example, the flash translation layer **600***a* may increase count values of sub blocks, not refreshed, from among sub blocks of the first memory block.

In operation S**970**, the flash translation layer **600***a* invalidates the first sub block. For example, the flash translation layer **600***a* invalidates refreshed sub blocks from among sub blocks of the first memory block.

If a count value of a sub block of the first memory block is smaller than the reference value TV, the flash translation layer **600***a* increases count values of sub blocks of the first memory block according to a program, read, or erase operation executed at one sub block of the first memory block.

FIG. **31** is a flowchart for describing a control method of FIG. **22** according to example embodiments of inventive concepts. Referring to FIGS. **1**, **21**, and **31**, in operation S**1010**, a flash translation layer **600***a* generates a program or read command associated with one sub block of sub blocks of a first memory block.

In operation S**1020**, the flash translation layer **600***a* judges whether a count value of a sub block of the first memory block is equal to or larger than a reference value TV.

If the count value of the first memory block is equal to or larger than the reference value TV, in operation S**1030**, the flash translation layer **600***a* sends a command for refreshing to a second memory block from a first sub block (e.g., a sub block having a count value that reaches the reference value TV) of the first memory block. In response to the refresh command, the nonvolatile memory device **100** performs reads data from the first sub block of the first memory block, and may reprogram a sub block of the second memory block with the read data.

In operation S**1040**, the flash translation layer **600***a* invalidates the first sub block (e.g., a sub block having a count value that reaches the reference value TV) of the first memory block.

In operation S**1050**, the flash translation layer **600***a* increases count values of sub blocks of the first memory block and the second memory block according to the refresh operation.

In operation S**1060**, there is judged whether a refreshed sub block is associated with the generated command. That is, there is judged whether a sub block corresponding to a program or read command is the refreshed sub block. If the refreshed sub block corresponds to the program or read command, in operation S**1070**, a program or read command associated with a sub block (e.g., a sub block corresponding to the command) of the second memory block is transferred to the nonvolatile memory device **100**. In operation S**1080**, count values of sub blocks of the second memory block are increased according to programming or reading.

If a sub block, having a count value reaching the reference value TV, from among sub blocks of the first memory block does not exist (S**1020**) or when the refreshed sub block does not correspond to a command (S**1060**), the flash translation layer **600***a* provides the nonvolatile memory device **100** with a program or read command associated with one sub block of the first memory block **100**. In operation S**1095**, the flash translation layer **600***a* increases count values of sub blocks of the first memory block according to programming or reading.

FIG. **32** is a flowchart for describing a control method of FIG. **22** according to example embodiments of inventive concepts. Referring to FIGS. **1**, **21**, and **32**, in operation S**1110**, a flash translation layer **600***a* generates an erase command on one sub block of sub blocks of a first memory block.

In operation S**1120**, the flash translation layer **600***a* judges whether a count value of a sub block of the first memory block is equal to or larger than a reference value TV. If a count value of a sub block of the first memory block is equal to or larger than a reference value TV, in operation S**1130**, there is judged whether a sub block having a count value equal to or larger than the reference value TV corresponds to the erase command. That is, whether a sub block having a count value over the reference value TV is a sub block to be erased may be judged.

If a sub block having a count value over the reference value TV is not a sub block to be erased, in operation S**1140**, there is transferred a command for refreshing to a second memory block from a first sub block (e.g., a sub block having a count value that reaches the reference value TV) of the first memory block. In response to the refresh command, the nonvolatile memory device **100** reads data from the first sub block to reprogram a sub block of the second memory block with the read data.

In operation S**1150**, the flash translation layer **600***a* sends an erase command associated with a sub block of the first memory block to the nonvolatile memory device **100**. In response to the erase command, the nonvolatile memory device **100** erases a sub block of the first memory block.

In operation S**1160**, the flash translation layer **600***a* increases count values of sub blocks of the first and second memory blocks according to the refresh operation.

In operation S**1170**, the flash translation layer **600***a* increases count values of sub blocks of the first memory block according to an erase operation.

In operation S**1180**, the flash translation layer **600***a* invalidates the first sub block of the first memory block.

If a sub block, having a count value larger than the reference value TV, from among sub blocks of the first memory block does not exist (S**1120**) or when a sub block having a count value larger than the reference value TV is a sub block to be erased (S**1130**), in operation S**1190**, the flash translation layer **600***a* provides the nonvolatile memory device **100** with an erase command associated with a sub block of the first memory block. In response to the erase command, the nonvolatile memory device **100** erases the sub block of the first memory block.

In operation S**1195**, the flash translation layer **600***a* increases count values of sub blocks of the first memory block according to the erase operation.

FIG. **33** is a flowchart for describing a control method of FIG. **22** according to example embodiments of inventive concepts. A control method in FIG. **33** is identical to that in FIG. **10** except that count values of sub blocks of a first memory block are increased according to a program, read, or erase operation (S**1230**) after a program, read, or erase command is transferred (S**1220**) and before a count value is compared with a reference value TV (S**1240**).

In the above-described embodiments, a sub block of a first memory block is reprogrammed to a sub block of a second memory block. However, a sub block of a first memory block can be reprogrammed to another sub block of the first memory block.

FIG. **34** is a flowchart for describing a control method of FIG. **22** according to example embodiments of inventive concepts. Referring to FIGS. **1**, **21**, and **34**, in operation S**1310**, a flash translation layer **600***a* generates a program, read, or erase command on one sub block of sub blocks of a memory block.

In operation S**1320**, the flash translation layer **600***a* provides a nonvolatile memory device **100** with a program, read, or erase command on a sub block of a memory block. In response to the command, the nonvolatile memory device **100** performs a program, read, or erase operation.

In operation S**1330**, the flash translation layer **600***a* judges whether a count value of a sub block of a memory block is equal to or larger than a reference value TV. If a count value of a sub block is over the reference value TV, in operation S**1340**, the flash translation layer **600***a* provides the nonvolatile memory device **100** with a reclaim command on a first sub block (e.g., a sub block having a count value that reaches the reference value TV) of the memory block. In response to the reclaim command, the nonvolatile memory device **100** performs a reclaim operation. That is, the nonvolatile memory device **100** reads data from the first sub block, erases the first sub block, and reprogram the first sub block with the read data.

In operation S**1350**, the flash translation layer **600***a* increases count values of sub blocks of the memory block according to a program, read, or erase operation and a reclaim operation.

If a sub block having a count value reaching the reference value TV does not exist (S**1330**), in operation S**1360**, the flash translation layer **600***a* increases count values of sub blocks of the memory block according to a program, read, or erase operation.

FIG. **35** is a flowchart for describing a control method of FIG. **22** according to example embodiments of inventive concepts. Referring to FIGS. **1**, **21**, and **35**, in operation S**1410**, a flash translation layer **600***a* generates a program or read command on one sub block of sub blocks of a memory block.

In operation S**1420**, the flash translation layer **600***a* judges whether a count value of a sub block of a memory block is equal to or larger than a reference value TV. If a count value of a sub block is over the reference value TV, in operation S**1430**, the flash translation layer **600***a* provides the nonvolatile memory device **100** with a reclaim command on a first sub block (e.g., a sub block having a count value that reaches the reference value TV) of the memory block. In response to the reclaim command, the nonvolatile memory device **100** performs a reclaim operation on the first sub block. The nonvolatile memory device **100** reads data from the first sub block, erases the first sub block, and reprogram the first sub block with the read data.

In operation S**1440**, the flash translation layer **600***a* provides the nonvolatile memory device **100** with a program or read command on a sub block of a memory block. In response to the command, the nonvolatile memory device **100** performs a program or read operation on the sub block of the memory block.

In operation S**1450**, the flash translation layer **600***a* increases count values of sub blocks of the memory block according to a program or read operation and a reclaim operation.

When a sub block having a count value reaching a reference value TV does not exist (S**1420**), in operation S**1460**, the flash translation layer **600***a* provides the nonvolatile memory device **100** with a program or read command of the sub block of the memory block. In response to the command, the nonvolatile memory device **100** performs a program or read operation on the sub block.

In operation S**1470**, the flash translation layer **600***a* increases count values of sub blocks of the memory block according to a program or read operation.

FIG. **36** is a flowchart for describing a control method of FIG. **22** according to example embodiments of inventive concepts. Referring to FIGS. **1**, **21**, and **36**, in operation S**1510**, a flash translation layer **600***a* generates an erase command on one sub block of sub blocks of a memory block.

In operation S**1520**, the flash translation layer **600***a* judges whether a count value of the sub block of the memory block is equal to or larger than a reference value TV. If a count value of the sub block is over the reference value TV, in operation S**1530**, the flash translation layer **600***a* judges whether a sub block having a count value over the reference value TV corresponds to an erase command. That is, there is judged whether a sub block having a count value over the reference value TV is a sub block to be erased. If a sub block having a count value over the reference value TV is not a sub block to be erased, in operation S**1540**, the flash translation layer **600***a* sends a reclaim command on a first sub block (e.g., a sub block having a count value reaching the reference value TV) of the memory block. In response to the reclaim command, the nonvolatile memory device **100** performs a reclaim operation on the first sub block of the memory block. For example, the nonvolatile memory device **100** reads data from the first sub block, erases the first sub block, and reprograms the first sub block with the read data.

In operation S**1550**, the flash translation layer **600***a* provides the nonvolatile memory device **100** with an erase command on a sub block of the memory block. In response to the erase command, the nonvolatile memory device **100** erases the sub block.

In operation S**1560**, the flash translation layer **600***a* increases count values of sub blocks of the memory block according to an erase operation and a reclaim operation.

When no sub block having a count value over the reference value TV exists (S**1520**) or when a sub block having a count value reaching the reference value TV is a sub block to be erased (S**1530**), in operation S**1570**, the flash translation layer **600***a* provides the nonvolatile memory device **100** with an erase command on a sub block of the memory block. In response to the erase command, the nonvolatile memory device **100** erases the sub block.

In operation S**1580**, the flash translation layer **600***a* increases count values of sub blocks of the memory block according to an erase operation.

FIG. **37** is a flowchart for describing a control method of FIG. **22** according to example embodiments of inventive concepts. Referring to FIGS. **1**, **21**, and **37**, in operation S**1610**, a flash translation layer **600***a* generates a program, read, or erase command on one sub block of sub blocks of a first memory block.

In operation S**1620**, the flash translation layer **600***a* provides the nonvolatile memory device **100** with a program, read, or erase command of the sub block of the memory device. In response to the sent command, the nonvolatile memory device **100** performs a program, read, or erase operation on the sub block.

In operation S**1630**, the flash translation layer **600***a* increases count values of sub blocks of the memory block according to a program, read, or erase operation.

In operation S**1640**, the flash translation layer **600***a* judges whether a count value of a sub block of the memory block is equal to or larger than a reference value TV. If a count value of a sub block of the memory block is smaller than the reference value TV, programming, reading, or erasing may be ended. If a count value of a sub block of the memory block is over the reference value TV, in operation S**1650**, the flash translation layer **600***a* provides the nonvolatile memory device **100** with a reclaim command on a first sub block (e.g., a sub block having a count value reaching the reference value TV) of the memory block. In response to the reclaim command, the nonvolatile memory device **100** performs a reclaim operation on the first sub block of the memory block. For example, the nonvolatile memory device **100** reads data from the first sub block, erases the first sub block, and reprograms the first sub block with the read data.

In operation S**1660**, the flash translation layer **600***a* increases count values of sub blocks of the memory block according to a reclaim operation.

As described above, the flash translation layer **600***a* manages a count value indicating disturb influence (e.g., disturb-generated number) by the sub block. If a count value of a specific sub block is equal to or larger than a reference value TV, the flash translation layer **600***a* controls the nonvolatile memory device **100** such that data of the specific sub block is reprogrammed in another sub block. Thus, it is possible to provide a control method of the nonvolatile memory device with improved reliability.

FIG. **38** is a circuit diagram schematically illustrating sub blocks, formed of memory cells in a memory block in FIG. **7**, according to example embodiments of inventive concepts. Referring to FIG. **38**, a common source line CSL is separated along a column direction. NAND strings NS in one row are connected to one common source line CSL. NAND strings NS in another row are connected to another command source line CSL. Memory cells MC in one row form a sub block. That is, sub blocks are formed by the row of a memory block BLKi+**1**.

A count value is managed by the memory block or by the sub block. Data is reprogrammed according to a count value.

FIG. **39** is a perspective view illustrating one of the memory blocks BLK**1** to BLKz of FIG. **3** according to example embodiments of inventive concepts. FIG. **40** is a sectional view taken along the line XL-XL' of a memory block of FIG. **39**.

Compared to the memory block BLKi described with reference to FIGS. **4** through **6**, provided are first conductive materials **211'** to **281'**, **212'** to **282'**, and **213'** to **283'** corresponding to first to eight heights, respectively. Insulation materials **112'** having greater thicknesses than insulation materials **112** are provided between the first conductive materials **241'**, **242'**, and **243'** having the fourth height and the first conductive materials **251'**, **252'**, and **253'** having the fifth height.

FIG. **41** is a circuit diagram illustrating an equivalent circuit of the memory block BLKj described with reference to FIGS. **39** and **40**. Referring to FIGS. **39** through **41**, the conductive materials **211'**, **212'**, and **213'** having the first height are commonly connected to form a ground selection line GSL.

The first conductive materials **221'** to **271'**, **222'** to **272'**, and **223'** to **273'** corresponding to the respectively second to seventh heights form first to sixth word lines WL**1** to WL**6**. The first conductive materials **281'**, **282'**, and **283'** having the eighth height form first to third string selection lines SSL**1**, SSL**2**, and SSL**3**.

Except for a change of the height, the first conductive materials **211'** to **281'**, **212'** to **282'**, and **213'** to **283'** form a ground selection line GSL, word lines WL**1** to WL**6**, and string selection lines SSL**1**, SSL**2**, and SSL**3**, as described with reference to FIGS. **4** through **4** through **6**. Accordingly, their detailed description is omitted.

The first to third memory cells MC**1** to MC**3** form a first sub block and the fourth to sixth memory cells MC**4** to MC**6** form a second sub block.

FIG. **42** is a table illustrating voltage conditions applied to the memory block BLKj_**1** of FIG. **41** during an erase operation. Referring to FIGS. **41** and **42**, string selection lines SSL**1** to SSL**3** float during an erase operation. Word lines WL of an unselected sub block float. A word line erase voltage Vwe is applied to word lines WL of a selected sub block. Then, an erase voltage Vers is applied to a substrate **111**.

For example, it is assumed that a first sub block is selected. During an erase operation, a word line erase voltage Vwe may be applied to word lines WL**1** to WL**3** of a selected first sub block. Also, during an erase operation, word lines WL**4** to WL**6** of an unselected second sub block may float.

FIG. **43** is a timing diagram illustrating a voltage change of the memory block BLKj_**1** of FIG. **41** according to a voltage condition of FIG. **42**. FIG. **44** is a sectional view illustrating one NAND string of the memory block BLKj_**1**. Hereinafter, with reference to a section of one NAND string NS shown in FIG. **44**, an erase operation of the memory block BLKj_**1** is described. For example, it is assumed that a first sub block is erased and a second sub block is erase-inhibited.

Referring to FIGS. **41** through **44**, an erase voltage Vers is applied to a substrate **111** at a first timing t**1**. For example, the erase voltage Vers is a high voltage.

The substrate **111** is doped with the same type as a surface layer **114** operating as a body of the second direction. Accordingly, the erase voltage Vers is delivered to the surface layer **114** of a NAND string NS.

As described with reference to FIGS. **9** through **11**, at the first timing t**1**, a ground selection line GSL floats. Accordingly, a ground selection transistor GST may be erase-inhibited.

At the first timing t**1**, a word line erase voltage Vwe is applied to selected word lines. Accordingly, first to third memory cells MC**1** to MC**3** of the selected first sub block may be erased.

At the first timing t**1**, unselected word lines float. Accordingly, fourth to sixth memory cells MC**4** to MC**6** of an unselected second sub block may be erase-inhibited.

At the first timing t**1**, a string selection line SSL floats. Accordingly, a string selection transistor SST may be erase-inhibited.

In addition, when a word line erase voltage Vwe is applied to word lines (e.g., WL**1** to WL**3**) of a selected sub block, a voltage of word lines (e.g., WL**4** to WL**6**) of a unselected sub block rises to an unselected word line voltage Vuwl by coupling. At this point, the word lines WL**4** to WL**6** of the unselected sub block may be affected by coupling from a word line erase voltage Vwe applied to the word lines WL**1** to WL**3** of a selected sub block. That is, due to the coupling from the word lines WL**1** to WL**3** of the selected sub block, a voltage rise width of the word lines WL**4** to WL**6** of an unselected sub block may be deteriorated. Moreover, a voltage of the word lines WL**1** to WL**3** of a selected sub block may rise by the coupling from the word lines WL**1** to WL**3** of the selected sub block.

Between the first sub block and the second sub block, an insulation material **112'** is provided. A thickness of the insulation material **112'** between the first and second sub blocks is greater than that of the insulation materials **112** between word lines WL in each sub block. That is, when it is assumed that a distance according to the second direction between memory cells MC in each sub block is a first distance, memory cells provided at an interface of sub blocks adjacent along a direction (i.e., the second direction) intersecting (for example, perpendicular to) a substrate are spaced apart from each other by a longer second distance than the first distance along the second direction and then are provided. In example embodiments, the insulation material **112'** acts as a separator to separate the first sub block from the second sub block

As the second distance is increased, influence of the coupling between sub blocks may be reduced. Therefore, this prevents a voltage rise width of the word lines WL**4** to WL**6** of an unselected sub block from being deteriorated. Moreover, this prevents a voltage of the word lines WL**1** to WL**3** of a selected sub block from rising. Additionally, as the second distance is increased, electric fields between sub blocks are distributed. Accordingly, hot carrier occurrence is prevented by electric fields between the word lines WL**1** to WL**3** of a selected sub block and the word lines WL**4** to WL**6** of an unselected sub block.

As mentioned above, the nonvolatile memory device **100** of FIGS. **1** and **2** according to example embodiments of inventive concepts performs an erase operation by a sub block unit. Accordingly, an operating speed of the nonvolatile memory device **100** may be improved. Additionally, an operating speed of a memory system **1000** including the nonvolatile memory device **100** may be improved.

As mentioned above, in the memory block BLKj_**1** of the nonvolatile memory device **1000** according to example embodiments of inventive concepts, a thickness of an insulation material **112'** between sub blocks is greater than that of an insulation material in each sub block. Therefore, the nonvolatile memory device **100** and the memory system **1000** including the nonvolatile memory device **100** become more reliable.

In the above-mentioned example embodiments, it is described that an erase voltage Vers and a word line erase voltage Vwe are applied at the first timing. However, the erase voltage Vers and the word line erase voltage Vwe may be sequentially applied according to a predetermined or desired order.

In the above-mentioned example embodiments, it is described that unselected word lines (e.g., WL4 to WL6) float. However, as shown in FIGS. 13 through 15, a word line erase-inhibit voltage Vwei may be applied to unselected word lines (e.g., WL4 to WL6).

FIG. 45 is a perspective view illustrating one among the memory blocks BLK1 to BLKz of FIG. 3 according to example embodiments of inventive concepts. FIG. 46 is a sectional view taken along the line III-III' of the memory block BLKm of FIG. 45.

Compared to the memory block BLKj described with reference to FIGS. 39 through 44, the first conductive materials 221", 222", and 223" having the second height and the first conductive materials 241", 242", and 243" having the fourth height in the first sub block have greater thicknesses than the remaining first conductive materials. Moreover, the first conductive materials 251", 252", and 253" having the fifth height and the first conductive materials 271", 272", and 273" having the seventh height in the second sub block have greater thicknesses than the remaining first conductive materials.

An equivalent circuit of the memory block BLKm is the same as the equivalent circuit BLKj_1 shown in FIG. 41. Voltage conditions applied to the memory block BLKm during an erase operation are the same as those shown in FIG. 42. Additionally, a voltage change of the memory block BLKm during an erase operation is the same as that shown in FIG. 43.

FIG. 47 is a sectional view illustrating one NAND string NS of the memory block BLKm. Hereinafter, an erase operation of the memory block BLKm is described with reference to FIGS. 42, 43, and 47. For example, it is assumed that a first sub block is erased and a second sub block is erase-inhibited.

During an erase operation, a word line erase voltage Vwe is applied to first to third word lines connected to first to third memory cells MC1 to MC3. An erase voltage Vers is applied to a surface layer 114 operating as a body of the second direction. The first to third memory cells MC1 to MC3 are erased by electric fields formed between the first to third memory cells MC1 to MC3 and the surface layer 114.

The third memory cell MC3 is provided at the top of the second memory cell MC2 and the first memory cell MC1 is provided at the bottom of the second memory cell MC2. According to influence of electric fields 1 and 3 generated between the first to third memory cells MC1 to MC3 and the surface layer 114, an electric field 2 generated between the second memory cell MC2 and the surface layer 114 is concentrated.

In addition, a ground selection transistor GST in a floating state is provided at the bottom of the first memory cell MC1. Accordingly, the electric field 1 between the first memory cells MC1 and the surface layer 114 is distributed in a direction of the ground selection transistor GST. Therefore, erase efficiency of the first memory cell MC1 may be lower than that of the second memory cell MC2.

A fourth memory cell MC4 in a floating state is provided at the top of the third memory cell MC3. Accordingly, the electric field 3 between the third memory cells MC3 and the surface layer 114 is distributed in a direction of the fourth memory cell MC4. Therefore, erase efficiency of the third memory cell MC3 may be lower than that of the second memory cell MC2.

According to example embodiments of inventive concepts, each of the first and last memory cells MC1 and MC3 has a first size and the remaining memory cell MC2 has a smaller second size than the first size, along a direction intersecting (for example, perpendicular to) a substrate 111 in each sub block. For example, the memory cells MC1 and MC3 provided at the outline of each sub block have a greater thickness than the memory cell MC2 provided within each sub block.

If the thickness of the first conductive material 221" having the second height is increased, a coupling ratio between the first conductive material 221" having the second height and the surface layer 114 is increased. Therefore, erase efficiency of the first memory cell MC1 may be improved.

Likewise, if the thickness of the first conductive material 241" having the fourth height is increased, a coupling ratio between the first conductive material 241" having the fourth height and the surface layer 114 is increased. Therefore, erase efficiency of the third memory cell MC3 may be improved.

Likewise, in the second sub block, the first and last memory cells MC4 and MC6 has a first size along a direction intersecting (for example, perpendicular to) the substrate 111 and the remaining memory cells MC5 has a smaller second size than the first size. Therefore, erase efficiency of the fourth and sixth memory cells MC4 and MC6 may be improved.

That is, by increasing the sizes of the memory cells MC1 and MC 3 provided at the end of each sub block, erase speeds of the memory cells MC1, MC2, and MC3 in each sub block are equalized. Therefore, since threshold voltage distribution of an erase state of the memory cells MC1, MC2, and MC3 is reduced, the nonvolatile memory device 100 and the memory system 1000 including the same become more reliable.

FIG. 48 is a perspective view illustrating one among the memory blocks BLK1 to BLKz of FIG. 3 according to example embodiments of inventive concepts. FIG. 49 is a sectional view taken along the line IV-IV' of the memory block BLKn of FIG. 48. Compared to the memory block BLKi described with reference to FIGS. 4 through 6, the first conductive materials 221", 222", and 223" having the second height and the first conductive materials 241", 242", and 243" having the fourth height in the first sub block of the memory block BLKn have greater thicknesses than the remaining first conductive materials. Moreover, the first conductive materials 251", 252", and 253" having the fifth height and the first conductive materials 271", 272", and 273" having the seventh height in the second sub block have greater thicknesses than the remaining first conductive materials.

An equivalent circuit of the memory block BLKn is the same as the equivalent circuit BLKj_1 shown in FIG. 8. Voltage conditions applied to the memory block BLKn during an erase operation are the same as those shown in FIG. 9 or 13. Additionally, a voltage change of the memory block BLKn during an erase operation is the same as that shown in FIG. 10 or 14.

As described with reference to FIGS. 45 through 47, each of the first and last memory cells MC1 and MC3 has a first size and the remaining memory cell MC2 has a smaller second size than the first size, along a direction intersecting (for example, perpendicular to) a substrate 111 in each sub block. For example, the memory cells MC1 and MC3 provided at the outline of each sub block have a greater thickness than the memory cell MC2 provided inside each sub block.

If the thickness of the first conductive material 221" having the second height is increased, a coupling ratio between the first conductive material 221" having the second height and the surface layer 114 is increased. Therefore, erase efficiency of the first memory cell MC1 may be improved.

Likewise, if the thickness of the first conductive material **241"** having the fourth height is increased, a coupling ratio between the first conductive material **241"** having the fourth height and the surface layer **114** is increased. Therefore, erase efficiency of the third memory cell MC**3** may be improved.

That is, by increasing the sizes of the memory cells MC**1** and MC**3** provided at the end of each sub block, erase speeds of the memory cells MC**1**, MC**2**, and MC**3** in each sub block are equalized. Therefore, since threshold voltage distribution of an erase state of the memory cells MC**1**, MC**2**, and MC**3** is reduced, the nonvolatile memory device **100** and the memory system **1000** including the same may become more reliable.

FIG. **50** is a circuit diagram illustrating an equivalent circuit BLKi_**2** of the memory block BLKi described with reference to FIGS. **4** and **6** according to example embodiments of inventive concepts. Compared to the equivalent circuit described with reference to FIG. **8**, a lateral transistor LTR is additionally provided at each NAND string NS of the memory block BLKi_**2**.

In each NAND string NS, the lateral transistor LTR is connected between a ground selection transistor GST and a common source line CSL. A gate (or a control gate) of the lateral transistor LTR and a gate (or control gate) of the ground selection transistor GST are connected to the ground selection line GSL.

As described with reference to FIGS. **4** through **7**, the first conductive materials **211**, **212**, and **213** having the first height correspond to first to third ground selection lines GSL**1** to GSL**3**, respectively.

Once a specific voltage is applied to the first conductive materials **211**, **212**, and **213** having the first height, a channel is formed in a region of the surface layer **114** adjacent to the first conductive materials **211**, **212**, and **213**. Moreover, if a specific voltage is applied to the first conductive materials **211**, **212**, and **213**, a channel is formed in a region of the substrate **111** adjacent to the first conductive materials **211**, **212**, and **213**.

A first doping region **311** is connected to a channel in the substrate **111**, which is formed by a voltage of the first conductive material. The channel of the substrate **111** generated by a voltage of the first conductive material **211** is connected to a channel formed by voltage of the first conductive material **211** in the surface layer **114** operating as a body of the second direction.

Likewise, a channel is formed in the substrate **111** by a voltage of the first conductive materials **211**, **212**, and **213**. First to fourth doping regions **311** to **314** are respectively connected to the surface layers **114** operating as a body of the second direction through a channel formed by a voltage of the first conductive materials **211**, **212**, and **213** in the substrate **111**.

As described with reference to FIGS. **4** through **7**, the first to fourth doping regions **311** to **314** are commonly connected to form a common source line CSL. The common source line CSL and the channels of the memory cells MC**1** to MC**6** are electrically connected through channels perpendicular and parallel to the substrate **111**, which are formed by a voltage of the ground selection line GSL.

That is, it is understood that transistors perpendicular and parallel to a substrate, driven by the ground selection line GSL, are provided between the common source line CSL and the first memory cells MC**1**. A transistor perpendicular to a substrate may be understood as a ground selection transistor GST and a transistor parallel to a substrate may be understood as a lateral transistor LST.

For example, as described with reference to FIGS. **39** through **44**, instead of providing dummy memory cells DMC between sub blocks, a thickness of the insulation material **112'** between sub blocks may be formed greater than those of other insulation materials **112**.

For example, as described with reference to FIGS. **45** through **47**, dummy memory cells DMC are not provided, and along a direction intersecting (for example, perpendicular to) the substrate **111** in each sub block, each of the first to last memory cells MC**1**, MC**3**, MC**4**, and MC**6** has a first size and each of the remaining memory cells MC**2** and MC**5** has a smaller second size than the first size.

For example, as described with reference to FIGS. **48** and **49**, dummy memory cells DMC are provided, and along a direction intersecting (for example, perpendicular to) the substrate **111** in each sub block, each of the first to last memory cells MC**1**, MC**3**, MC**4**, and MC**6** has a first size and each of the remaining memory cells MC**2** and MC**5** has a smaller second size than the first size.

For example, as described with reference to FIGS. **18** through **20**, while a read operation is performed on a selected sub block among sub blocks of the memory block BLKi_**2**, each sub block of the memory block BLKi_**2** is selectively refreshed. For example, after data are written on a specific sub block of the memory block BLKi_**2**, when the number of reading operations on sub blocks of the memory block BLKi_**2** reaches a reference value, a specific sub block is refreshed.

As described in relation to FIGS. **21** to **38**, a refresh operation or a reclaim operation may be carried out by the memory block or the sub block.

FIG. **51** is a circuit diagram illustrating an equivalent circuit BLKi_**3** of the memory block BLKi described with reference to FIGS. **4** and **6** according to example embodiments of inventive concepts. Compared to the equivalent circuit described with reference to FIG. **8**, two ground selection transistors GST**1** and GST**2** may be provided between the memory cells MC**1** to MC**4** and the common source line CSL in each NAND string NS. The ground selection lines GSL**1** and GSL**2** corresponding to the ground selection transistor GST**1** or GST**2** having the same height may be commonly connected. Moreover, the ground selection lines GSL**1** and GSL**2** corresponding to the same NAND string NS may be commonly connected.

For example, in order to equalize the number of memory cells of the first and second sub blocks, the number of dummy word lines DWL**1** and DWL**2** and dummy memory cells DMC**1** and DMC**2** is adjusted. The number of the memory cells MC**1** and MC**2** of the first sub block and the memory cells MC**3** and MC**4** of the second sub block is not limited to FIG. **51**.

For example, as described with reference to FIGS. **39** through **44**, instead of providing dummy memory cells DMC between sub blocks, a thickness of the insulation material **112'** between sub blocks may be formed greater than those of other insulation materials **112**.

For example, as described with reference to FIGS. **45** through **47**, dummy memory cells DMC are not provided, and along a direction intersecting (for example, perpendicular to) the substrate **111** in each sub block, each of the first to last memory cells MC**1**, MC**2**, MC**3**, and MC**4** has a first size and each of the remaining memory cells (not shown) has a smaller second size than the first size.

For example, as described with reference to FIGS. **48** and **49**, the dummy memory cells DMC**1** and DMC**2** are provided, and along a direction intersecting (for example, perpendicular to) the substrate **111** in each sub block, each of the first to last memory cells MC**1**, MC**2**, MC**3**, and MC**4** has a first size and each of the remaining memory cells (not shown) has a smaller second size than the first size.

For example, as described with reference to FIGS. **18** through **20**, while a read operation is performed on a selected sub block among sub blocks of the memory block BLKi_3, each sub block of the memory block BLKi_3 is selectively refreshed. For example, after data are written on a specific sub block of the memory block BLKi_3, when the number of reading operations on sub blocks of the memory block BLKi_3 reaches a reference value, a specific sub block is refreshed.

As described in relation to FIGS. **21** to **38**, a refresh operation or a reclaim operation may be carried out by the memory block or the sub block.

FIG. **52** is a circuit diagram illustrating an equivalent circuit BLKi_**4** of the memory block BLKi described with reference to FIGS. **4** and **6** according to example embodiments of inventive concepts. Compared to the memory block BLKi_3 of FIG. **51**, two string selection transistors SSTa and SSTb may be provided between the memory cells MC**1** to MC**4** and the bit line BL.

In NAND strings in the same row, the string selection transistor SSTa or SSTb having the same height may share one string selection line SSL. For example, in the NAND strings NS**11** to NS**13** of a first row, the a string selection transistors SSTa share a **1***a* string selection line SSL**1***a*. The b string selection transistors SSTb share a **1***b* string selection line SSL**1***b*.

In NAND strings NS**21** to NS**23** in the second row, the a string selection transistors SSTa share a **2***a* string selection line SSL**2***a*. The b string selection transistors SSTb share a **2***b* string selection line SSL**2***b*.

In NAND strings NS**21** to NS**23** in the third row, the string selection transistors SSTa share a **3***a* string selection line SSL**3***a*. The b string selection transistors SSTb share a **3***b* string selection line SSL**3***b*.

As mentioned with reference to FIG. **51**, the number of dummy word lines DWL and dummy memory cells DMC provided between sub blocks, the number of memory cells MC**1** and MC**2** of the first sub block, and the number of the memory cells MC**3** and MC**4** of the second sub block are not limited.

For example, as described with reference to FIGS. **39** through **44**, instead of providing dummy memory cells DMC between sub blocks, a thickness of the insulation material **112'** between sub blocks may be formed greater than those of other insulation materials **112**.

For example, as described with reference to FIGS. **45** through **47**, dummy memory cells DMC are not provided, and along a direction intersecting (for example, perpendicular to) the substrate **111** in each sub block, each of the first to last memory cells MC**1**, MC**2**, MC**3**, and MC**4** has a first size and each of the remaining memory cells (not shown) has a smaller second size than the first size.

For example, as described with reference to FIGS. **48** and **49**, the dummy memory cells DMC**1** and DMC**2** are provided, and along a direction intersecting (for example, perpendicular to) the substrate **111** in each sub block, each of the first to last memory cells MC**1**, MC**2**, MC**3**, and MC**4** has a first size and each of the remaining memory cells (not shown) has a smaller second size than the first size.

For example, as described with reference to FIGS. **18** through **20**, while a read operation is performed on a selected sub block among sub blocks of the memory block BLKi_**4**, each sub block of the memory block BLKi_**4** is selectively refreshed. For example, after data are written on a specific sub block of the memory block BLKi_**4**, when the number of reading operations on sub blocks of the memory block BLKi_**4** reaches a reference value, a specific sub block is refreshed.

As described in relation to FIGS. **21** to **38**, a refresh operation or a reclaim operation may be carried out by the memory block or the sub block.

FIG. **53** is a circuit diagram illustrating an equivalent circuit BLKi_**5** of the memory block BLKi described with reference to FIGS. **4** and **6** according to example embodiments of inventive concepts. Compared to the memory block BLKi_**4** of FIG. **52**, string selection lines SSL corresponding to the NAND strings NS of the same row are commonly connected.

As mentioned with reference to FIG. **51**, the number of dummy word lines DWL and dummy memory cells DMC provided between sub blocks, the number of memory cells MC**1** and MC**2** of the first sub block, and the number of the memory cells MC**3** and MC**4** of the second sub block are not limited.

For example, as described with reference to FIGS. **39** through **44**, instead of providing dummy memory cells DMC between sub blocks, a thickness of the insulation material **112'** between sub blocks may be formed greater than those of other insulation materials **112**.

For example, as described with reference to FIGS. **45** through **47**, dummy memory cells DMC are not provided, and along a direction intersecting (for example, perpendicular to) the substrate **111** in each sub block, each of the first to last memory cells MC**1**, MC**2**, MC**3**, and MC**4** has a first size and each of the remaining memory cells (not shown) has a smaller second size than the first size.

For example, as described with reference to FIGS. **48** and **49**, the dummy memory cells DMC**1** and DMC**2** are provided, and along a direction intersecting (for example, perpendicular to) the substrate **111** in each sub block, each of the first to last memory cells MC**1**, MC**2**, MC**3**, and MC**4** has a first size and each of the remaining memory cells (not shown) has a smaller second size than the first size.

For example, as described with reference to FIGS. **18** through **20**, while a read operation is performed on a selected sub block among sub blocks of the memory block BLKi_**5**, each sub block of the memory block BLKi_**5** is selectively refreshed. For example, after data are written on a specific sub block of the memory block BLKi_**5**, when the number of reading operations on sub blocks of the memory block BLKi_**5** reaches a reference value, a specific sub block is refreshed.

As described in relation to FIGS. **21** to **38**, a refresh operation or a reclaim operation may be carried out by the memory block or the sub block.

FIG. **54** is a circuit diagram illustrating an equivalent circuit BLKi_**6** of the memory block BLKi described with reference to FIGS. **4** and **6** according to example embodiments of inventive concepts. Compared to the memory block BLKi_**1** of FIG. **8**, the dummy memory cell DMC**3** is provided between the string selection transistor SST and the memory cells MC**1** to MC**4** in each NAND string NS. The dummy memory cells DMC**3** are commonly connected to the dummy word lines DWL**3**. That is, the dummy word line DWL**3** is provided between the string selection lines SSL**1** to SSL**3** and the word lines WL**1** to WL**4**.

As mentioned with reference to FIG. **51**, the number of dummy word lines DWL**1** and DWL**2** and dummy memory cells DMC**1** and DMC**2** provided between sub blocks, the number of memory cells MC**1** and MC**2** of the first sub block, and the number of the memory cells MC**3** and MC**4** of the second sub block are not limited. Likewise, the number of the dummy memory cells DMC**3** provided between the memory cells MC**1** to MC**4** and the string selection transistors SST is not limited.

For example, as described with reference to FIGS. **39** through **44**, instead of providing dummy memory cells DMC**1** and DMC**2** between sub blocks, a thickness of the insulation material **112'** between sub blocks may be formed greater than those of other insulation materials **112**.

For example, as described with reference to FIGS. **45** through **47**, dummy memory cells DMC**1** and DAM**2** are not provided, and along a direction intersecting (for example, perpendicular to) the substrate **111** in each sub block, each of the first to last memory cells MC**1**, MC**2**, MC**3**, and MC**4** has a first size and each of the remaining memory cells (not shown) has a smaller second size than the first size.

For example, as described with reference to FIGS. **48** and **49**, the dummy memory cells DMC**1** and DMC**2** are provided, and along a direction intersecting (for example, perpendicular to) the substrate **111** in each sub block, each of the first to last memory cells MC**1**, MC**2**, MC**3**, and MC**4** has a first size and each of the remaining memory cells (not shown) has a smaller second size than the first size.

For example, as described with reference to FIGS. **18** through **20**, while a read operation is performed on a selected sub block among sub blocks of the memory block BLKi_**6**, each sub block of the memory block BLKi_**6** is selectively refreshed. For example, after data are written on a specific sub block of the memory block BLKi_**6**, when the number of reading operations on sub blocks of the memory block BLKi_**6** reaches a reference value, a specific sub block is refreshed.

As described in relation to FIGS. **21** to **38**, a refresh operation or a reclaim operation may be carried out by the memory block or the sub block.

FIG. **55** is a circuit diagram illustrating an equivalent circuit BLKi_**7** of the memory block BLKi described with reference to FIGS. **4** and **6** according to example embodiments of inventive concepts. Compared to the memory block BLKi_**1** of FIG. **8**, the dummy memory cell DMC**1** is provided between the ground selection transistor GST and the memory cells MC**1** to MC**6** in each NAND string NS. The dummy memory cells DMC**1** are commonly connected to the dummy word lines DWL**3**. That is, the dummy word line DWL**1** is provided between the ground selection line GSL and the word lines WL**1** to WL**4**.

As mentioned with reference to FIG. **51**, the number of dummy word lines DWL**2** and DWL**3** and dummy memory cells DMC**2** and DMC**3** provided between sub blocks, the number of memory cells MC **1** and MC**2** of the first sub block, and the number of the memory cells MC**3** and MC**4** of the second sub block are not limited. Likewise, the number of the dummy memory cells DMC**1** provided between the memory cells MC**1** to MC**4** and the ground selection transistors GST is not limited.

For example, as described with reference to FIGS. **39** through **44**, instead of providing dummy memory cells DMC**2** and DMC**3** between sub blocks, a thickness of the insulation material **112'** between sub blocks may be formed greater than those of other insulation materials **112**.

For example, as described with reference to FIGS. **45** through **47**, dummy memory cells DMC**2** and DAM**3** are not provided, and along a direction intersecting (for example, perpendicular to) the substrate **111** in each sub block, each of the first to last memory cells MC**1**, MC**2**, MC**3**, and MC**4** has a first size and each of the remaining memory cells (not shown) has a smaller second size than the first size.

For example, as described with reference to FIGS. **48** and **49**, the dummy memory cells DMC**2** and DMC**3** are provided, and along a direction intersecting (for example, perpendicular to) the substrate **111** in each sub block, each of the first to last memory cells MC**1**, MC**2**, MC**3**, and MC**4** has a first size and each of the remaining memory cells (not shown) has a smaller second size than the first size.

For example, as described with reference to FIGS. **18** through **20**, while a read operation is performed on a selected sub block among sub blocks of the memory block BLKi_**7**, each sub block of the memory block BLKi_**7** is selectively refreshed. For example, after data are written on a specific sub block of the memory block BLKi_**7**, when the number of reading operations on sub blocks of the memory block BLKi_**7** reaches a reference value, a specific sub block is refreshed.

As described in relation to FIGS. **21** to **38**, a refresh operation or a reclaim operation may be carried out by the memory block or the sub block.

FIG. **56** is a circuit diagram illustrating an equivalent circuit BLKi_**8** of the memory block BLKi described with reference to FIGS. **4** and **6** according to example embodiments of inventive concepts. Compared to the memory block BLKi_**1** of FIG. **8**, the dummy memory cell DMC**1** is provided between the ground selection transistor GST and the memory cells MC**1** to MC**4** in each NAND string NS. The dummy memory cells DMC**1** are commonly connected to the dummy word lines DWL**1**. That is, the dummy word line DWL**1** is provided between the ground selection line GSL and the word lines WL**1** to WL**4**.

A dummy memory cell DMC**3** is provided between the string selection transistor SST and the memory cells MC**1** to MC**4** in each NAND string. The dummy memory cells DMC**3** are commonly connected to the dummy word line DWL**3**. That is, the dummy word line DWL**3** is provided between the string selection lines SSL**1** to SSL**3** and the word lines WL**1** to WL**6**.

As mentioned with reference to FIG. **51**, the number of dummy word lines DWL**2** and DWL**3** and dummy memory cells DMC**2** and DMC**3** provided between sub blocks, the number of memory cells MC**1** and MC**2** of the first sub block, and the number of the memory cells MC**3** and MC**4** of the second sub block are not limited. Likewise, the number of the dummy memory cells DMC**1** provided between the memory cells MC**1** to MC**4** and the ground selection transistors GST is not limited. Moreover, the number of the dummy memory cells DMC**3** provided between the memory cells MC**1** to MC**4** and the string selection transistors GST is not limited.

For example, as described with reference to FIGS. **39** through **44**, instead of providing dummy memory cells DMC**2** between sub blocks, a thickness of the insulation material **112'** between sub blocks may be formed greater than those of other insulation materials **112**.

For example, as described with reference to FIGS. **45** through **47**, dummy memory cells DMC**2** are not provided, and along a direction intersecting (for example, perpendicular to) the substrate **111** in each sub block, each of the first to last memory cells MC**1**, MC**2**, MC**3**, and MC**4** has a first size and each of the remaining memory cells (not shown) has a smaller second size than the first size.

For example, as described with reference to FIGS. **48** and **49**, the dummy memory cells DMC**2** are provided, and along a direction intersecting (for example, perpendicular to) the substrate **111** in each sub block, each of the first to last memory cells MC**1**, MC**2**, MC**3**, and MC**4** has a first size and each of the remaining memory cells (not shown) has a smaller second size than the first size.

For example, as described with reference to FIGS. **18** through **20**, while a read operation is performed on a selected sub block among sub blocks of the memory block BLKi_**8**, each sub block of the memory block BLKi_**8** is selectively refreshed. For example, after data are written on a specific sub block of the memory block BLKi_**8**, when the number of reading operations on sub blocks of the memory block BLKi_**8** reaches a reference value, a specific sub block is refreshed.

As described in relation to FIGS. **21** to **38**, a refresh operation or a reclaim operation may be carried out by the memory block or the sub block.

FIG. **57** is a perspective view of one of the memory blocks BLK**1**-BLKz according to example embodiments of inventive concepts. FIG. **58** is a cross-sectional view taken along the line LVIII-LVIII' of the memory block BLKo of FIG. **57**. Compared with the memory block BLKi described with reference to FIGS. **4** through **6**, one pillar in the memory block BLKo includes a first sub-pillar **113***a* and a second sub-pillar **113***b*. Except that the pillar **113** of the memory block BLKi is replaced by the first and second pillars **113***a*, **113***b*, the memory block BLKo has the same structure as the memory block BLKi. Therefore, repeated description will be omitted.

Referring to FIGS. **57** and **40**, the first sub-pillar **113***a* is provided on a substrate **111**. Exemplarily, a surface layer **114***a* of the first sub-pillar **113***a* includes a p-type silicon material. The surface layer **114***a* of the first sub pillar **113***a* functions as a body of the second direction. An inner layer of the first sub-pillar **113***a* is made of an insulation material.

The second sub-pillar **113***b* is provided on the first sub-pillar **113***a*. Exemplarily, a surface layer **114***b* of the second sub-pillar **113***b* includes a p-type silicon material. The surface layer **114***b* of the second sub-pillar **113***b* functions as a body in the second direction. An inner layer **115***b* of the second sub-pillar **113***b* is made of an insulation material.

Exemplarily, the surface layer **114***a* of the first sub-pillar **113***a* is connected to the surface layer **114***b* of the second sub-pillar **113***b*. For example, as shown in FIGS. **57** and **58**, the surface layer **114***a* of the first sub pillar **113***a* and the surface layer **114***b* of the second sub pillar **113***b* are connected through a p-type silicon pad SIP.

In a region having the silicon pad SIP, the surface layer **114***a* of the first sub pillar **113***a* and the surface layer **114***b* of the second sub pillar **113***b* are connected in an irregular form. Accordingly, in a region where the silicon pad SIP is provided, channel formation may be unstable. That is, memory cells MC having a height corresponding to the silicon pad SIP may not store, erase, or read data normally.

In order to prevent the above limitations, first conductive materials **251**, **252**, and **253** having a height corresponding to the silicon pad SIP (i.e., a fifth height) form a dummy word line DWL and a dummy memory cell DMC. That is, the memory block BLKo may be divided into sub blocks based on a height corresponding to the silicon pad SIP.

Exemplarily, an equivalent circuit of the memory block BLKo may be illustrated as the equivalent circuit BLKi_**1** shown in FIG. **8**. Exemplarily, an equivalent circuit of the memory block BLKo may be illustrated as the equivalent circuits BLKi_**2** to BLKi_**8** shown in FIGS. **50** through **56**. That is, each NAND string of the memory block BLKo may include a lateral transistor LTR. At least one dummy memory cell DMC may be provided between sub blocks of the memory block BLKo. The number of memory cells DMC, which may be further provided between sub blocks of the memory block BLKo, may vary.

In each NAND string, at least two string selection transistors SST may be provided. In each NAND sting, at least two ground selection transistors GST may be provided. In each NAND string, at least one dummy memory cell DMC may be provided between the memory cells MC and the string selection transistor SST. In each NAND string, at least one dummy memory cell DMC may be provided between the memory cells MC and the ground selection transistor GST.

Exemplarily, as described with reference to FIGS. **48** and **49**, along the direction intersecting (for example, perpendicular to) the substrate **111** in each sub block, each of the first to last memory cells MC**1**, MC**3**, MC**4**, and MC**6** has a first size and each of the remaining memory cells MC**2** and MC**5** has a smaller second size than the first size.

For example, as described with reference to FIGS. **18** through **20**, while a read operation is performed on a selected sub block among sub blocks of the memory block BLKi_o, each sub block of the memory block BLKi_o is selectively refreshed. For example, after data are written on a specific sub block of the memory block BLKi_o, when the number of reading operations on sub blocks of the memory block BLKi_o reaches a reference value, a specific sub block is refreshed.

As described in relation to FIGS. **21** to **38**, a refresh operation or a reclaim operation may be carried out by the memory block or the sub block.

Exemplarily, it is described that a pillar includes a first sub pillar **113***a* and a second sub pillar **113***b*. However, a pillar may include at least two sub pillars.

FIG. **59** is a perspective view of one of the memory blocks BLK**1**-BLKz according to example embodiments BLKi' of inventive concepts. A cross-sectional view taken along the line V-V' of the memory block BLKi' is the same as that of FIG. **4**.

Compared to the memory block BLKi of FIG. **4**, in the memory block BLKi, pillars **113'** has a square pillar form. Moreover, between the pillars **113'** spaced from each other along the first direction by a specific distance, insulation materials **101** are provided. Exemplarily, the insulation materials **101** extend along the second direction and contact the substrate **111**.

The first conductive materials **211** to **291**, **212** to **292**, and **213** to **293** described with reference to FIG. **4** are divided into first portions **211***a* to **291***a*, **212***a* to **292***a*, and **213***a* to **293***a* and second portions **211***b* to **291***b*, **212***b* to **292***b*, and **213***b* to **293***b* in a region including the insulation materials **101**.

In a region on first and second doping regions **311** and **312**, each pillar **113'** forms the first portions **211***a* to **291***a* and insulation layer **116** of the first conductive materials and one NAND string NS and forms the second portions **211***b* to **291***b* and insulation layer **116** of the first conductive materials and another NAND string NS.

In a region on second and third doping regions **312** and **313**, each pillar **113'** forms the first portions **212***a* to **292***a* and insulation layer **116** of the first conductive materials and one NAND string NS and forms the second portions **212***b* to **292***b* and insulation layer **116** of the first conductive materials and another NAND string NS.

In a region on third and fourth doping regions **313** and **314**, each pillar **113'** forms the first portions **213***a* to **293***a* and insulation layer **116** of the first conductive materials and one NAND string NS and forms the second portions **213***b* to **293***b* and insulation layer **116** of the first conductive materials and another NAND string NS.

That is, the first and second portions **211***a* to **291***a* and **211***b* to **291***b* of the first conductive materials provided at the both sides of each pillar **113'** are separated using the insulation material **101**, such that each pillar **113'** may form two NAND strings.

As described with reference to FIGS. **4** through **8**, the first portions **211***a* to **291***a* and the second portions **211***b* to **291***b*, **212***b* to **292***b*, and **213***b* to **293***b* of the first conductive materials may correspond to ground selection lines GSL, word lines WL, and string selection lines SST, respectively. The word lines WL having the same height are commonly connected.

Exemplarily, an equivalent circuit of the memory block BLKi' may be illustrated as the equivalent circuit BLKi_**1** shown in FIG. **8** except the number of rows in the NAND strings NS. For example, the number of rows in the NAND strings NS of an equivalent circuit of the memory block BLKi' may be two times that in the NAND strings NS of the equivalent circuit BLKi_**1** shown in FIG. **8**.

Exemplarily, an equivalent circuit of the memory block BLKi' may be illustrated as the equivalent circuits BLKi_**2** to BLKi_**8** shown in FIGS. **50** through **56** except the number of rows in the NAND strings NS. For example, the number of rows in the NAND strings NS of an equivalent circuit of the memory block BLKi' may be two times that in the NAND strings NS of the equivalent circuits BLKi_**2** to BLKi_**8** shown in FIGS. **50** through **56**.

Each NAND string of the memory block BLKi' may include a lateral transistor LTR. At least one dummy memory cell DMC may be provided between sub blocks of the memory block BLKi'. The number of memory cells DMC, which may be further provided between sub blocks of the memory block BLKi', may vary.

In each NAND string, at least two string selection transistors SST may be provided. In each NAND sting, at least two ground selection transistors GST may be provided. In each NAND string, at least one dummy memory cell DMC may be provided between the memory cells MC and the string selection transistor SST. In each NAND string, at least one dummy memory cell DMC may be provided between the memory cells MC and the ground selection transistor GST.

For example, as described with reference to FIGS. **39** through **44**, instead of providing dummy memory cells DMC between sub blocks, a thickness of the insulation material **112'** between sub blocks may be formed greater than those of other insulation materials **112**.

For example, as described with reference to FIGS. **45** through **47**, dummy memory cells DMC are not provided, and along a direction intersecting (for example, perpendicular to) the substrate **111** in each sub block, each of the first to last memory cells MC**1**, MC**3**, MC**4**, and MC**6** has a first size and each of the remaining memory cells MC**2** and MC**5** has a smaller second size than the first size.

For example, as described with reference to FIGS. **48** and **49**, along a direction intersecting (for example, perpendicular to) the substrate **111** in each sub block, each of the first to last memory cells MC**1**, MC**3**, MC**4**, and MC**6** has a first size and each of the remaining memory cells MC**2** and MC**5** has a smaller second size than the first size.

For example, as described with reference to FIGS. **18** through **20**, while a read operation is performed on a selected sub block among sub blocks of the memory block BLKi', each sub block of the memory block BLKi' is selectively refreshed. For example, after data are written on a specific sub block of the memory block BLKi', when the number of reading operations on sub blocks of the memory block BLKi' reaches a reference value, a specific sub block is refreshed.

As described in relation to FIGS. **21** to **38**, a refresh operation or a reclaim operation may be carried out by the memory block or the sub block.

FIG. **60** is a perspective view of one of the memory blocks BLK**1**-BLKz according to example embodiments of inventive concepts. A cross-sectional view taken along the line LVIII-LVIII' of the memory block BLKo' is the same as that of FIG. **58**.

As described with reference to FIGS. **57** and **58**, one pillar in the memory block BLKo' includes a first sub-pillar **113***a* and a second sub-pillar **113***b*. Except that a pillar has a square pillar form, the first sub pillars **113***a* and the second sub pillars **113***b* are the same as those described with reference to FIGS. **57** and **58**.

As illustrated with reference to FIG. **59**, one pillar **113'** forms two NAND string NS. The first portions **211***a* to **291***a* and the second portions **211***b* to **291***b*, **212***b* to **292***b*, and **213***b* to **293***b* of the first conductive materials may correspond to ground selection lines GSL, word lines WL, and string selection lines SST, respectively. The word lines WL having the same height are commonly connected.

Exemplarily, an equivalent circuit of the memory block BLKo' may be illustrated as the equivalent circuit BLKi_**1** shown in FIG. **8** except the number of rows in the NAND strings NS. For example, the number of rows in the NAND strings NS of an equivalent circuit of the memory block BLKo' may be two times that in the NAND strings NS of the equivalent circuit BLKi_**1** shown in FIG. **8**.

Exemplarily, an equivalent circuit of the memory block BLKo' may be illustrated as the equivalent circuits BLKi_**2** to BLKi_**8** shown in FIGS. **50** through **56** except the number of rows in the NAND strings NS. For example, the number of rows in the NAND strings NS of an equivalent circuit of the memory block BLKo' may be two times that in the NAND strings NS of the equivalent circuits BLKi_**2** to BLKi_**8** shown in FIGS. **50** through **56**.

Each NAND string of the memory block BLKo' may include a lateral transistor LTR. At least one dummy memory cell DMC may be provided between sub blocks of the memory block BLKo'. The number of memory cells DMC, which may be further provided between sub blocks of the memory block BLKo', may vary.

In each NAND string, at least two string selection transistors SST may be provided. In each NAND sting, at least two ground selection transistors GST may be provided. In each NAND string, at least one dummy memory cell DMC may be provided between the memory cells MC and the string selection transistor SST. In each NAND string, at least one dummy memory cell DMC may be provided between the memory cells MC and the ground selection transistor GST.

For example, as described with reference to FIGS. **48** and **49**, along a direction intersecting (for example, perpendicular to) the substrate **111** in each sub block, each of the first to last memory cells MC**1**, MC**3**, MC**4**, and MC**6** has a first size and each of the remaining memory cells MC**2** and MC**5** has a smaller second size than the first size.

As described with reference to FIGS. **57** and **58**, first conductive materials **251**, **252**, and **253** having a height corresponding to the silicon pad SIP (i.e., a fifth height) form a dummy word line DWL and a dummy memory cell DMC. That is, the memory block BLKo may be divided into sub blocks based on a height corresponding to the silicon pad SIP.

For example, as described with reference to FIGS. **18** through **20**, while a read operation is performed on a selected sub block among sub blocks of the memory block BLKo', each sub block of the memory block BLKo' is selectively refreshed. For example, after data are written on a specific sub block of the memory block BLKi_o, when the number of reading operations on sub blocks of the memory block BLKi_o reaches a reference value, a specific sub block is refreshed.

As described in relation to FIGS. 21 to 38, a refresh operation or a reclaim operation may be carried out by the memory block or the sub block.

Exemplarily, it is described that a pillar includes a first sub pillar 113*a* and a second sub pillar 113*b*. However, a pillar may include at least two sub pillars.

FIG. 61 is a perspective view of one of the memory blocks BLK1-BLKz according to example embodiments BLKp of inventive concepts. FIG. 62 is a sectional view taken along the line LVII-LXII' of the memory block BLKp of FIG. 61. Except that an n-type doping region 315 forming a common source line CSL is provided with a plate form, the memory block BLKp has the same configuration as the memory block BLKi described with reference to FIGS. 4 through 8. For example, an n-type doping region 315 may be provided as an n-type well.

As described with reference to FIGS. 4 through 8, the first conductive materials 211 to 291, 212 to 292, and 213 to 293 may correspond to ground selection lines GSL, word lines WL, and string selection lines SST, respectively. The word lines WL having the same height are commonly connected.

FIG. 63 is a table illustrating example embodiments of voltage conditions during an erase operation of the memory block BLKp of FIGS. 61 and 62. Referring to FIGS. 61 and 62, a string selection line SSL floats during an erase operation. Word lines WL of an unselected sub block float. Word lines WL of a selected sub block is driven by a second word line erase voltage Vwe2 after floating. A third dummy word line voltage Wdwl3 is applied to a dummy word line DWL. After a ground selection line GSL is driven by a ground voltage, it floats. Then, after a substrate 111 is driven by a pre voltage Vpre, it is driven by a second erase voltage Vers2.

FIG. 64 is a timing diagram illustrating a voltage change of the memory block BLKp of FIGS. 61 and 62 according to the voltage conditions of FIG. 63. Exemplarily, an equivalent circuit of the memory block BLKp may be illustrated as the equivalent circuit BLKi_1 shown in FIG. 8. Hereinafter, with reference to the equivalent circuit BLKi_1 of FIG. 8 and FIGS. 61 through 64, an erase operation of the memory block BLKp is illustrated. Exemplarily, it is assumed that a first sub block is erased and a second sub block is erase-inhibited.

At a first timing t1, a pre voltage Vpre is applied to a substrate 111. For example, the substrate 111 includes a p-type silicon material and a doping region 315 includes an n-type silicon material. Since the substrate 111 and the doping region 315 form a forward bias condition, a pre voltage Vpre is delivered to the doping region 315 through the substrate 111. For example, the pre voltage Vpre is a high voltage.

At a first timing t1, a ground voltage Vss is applied to the ground selection line GSL. A ground voltage is applied to a gate (or a control gate) of the ground selection transistor GST, and a pre voltage Vpre is applied to a source. Since a pre voltage Vpre is a high voltage, thermo electrons occur at the ground selection transistor GST. For example, thermo electrons occur by a gate induced drain leakage (GIDL) at the ground selection transistor GST. The generated thermo electrons are delivered from the doping region 315 to the surface layer 114 operating as a body of the second direction. Accordingly, a voltage of the surface layer 114 rises.

At a first timing t1, the word lines WL1 to WL3 of a selected sub block and the word line WL4 to WL6 of an unselected sub block float. Accordingly, voltages of the word lines WL1 to WL3 of a selected sub block and the word line WL4 to WL6 of an unselected sub block are raised by coupling according to voltage rise of the surface layer 114.

At a first timing t1, a third dummy word line voltage Vdwl3 is applied to the dummy word line DWL.

At a first timing t1, the string selection line SSL floats. Accordingly, a voltage of the string selection line SSL is raised by coupling according to voltage rise of the surface layer 114.

At a second timing t2, a second erase voltage Vers2 is applied to the substrate 111. The second erase voltage Vers2 is delivered to the doping region 315. Due to a difference between the second erase voltage Vers2 and a voltage of the ground selection line GSL, thermo electrons occur in the ground selection transistor GST. For example, thermo electrons may occur by GIDL in the ground selection transistor GST. The generated thermo electrons are injected on the surface layer 114 such that a voltage of the surface layer 114 may rise.

At a second timing t2, the ground selection line GSL floats. Accordingly, by coupling according to voltage rise of the surface layer 114, a voltage of the ground selection line GSL may rise. For example, a voltage of the ground selection line GSL rises up to the second ground selection line voltage Vgsl2.

At a second timing t2, the word lines WL1 to WL3 of a selected sub block and the word line WL4 to WL6 of an unselected sub block float. Accordingly, voltages of the word lines WL1 to WL3 of a selected sub block and the word line WL4 to WL6 of an unselected sub block are raised by coupling according to voltage rise of the surface layer 114. For example, voltages of the word lines WL1 to WL3 of a selected sub block and the word line WL4 to WL6 of an unselected sub block rise up to a word line voltage Vwl.

At a second timing t2, the string selection line SSL floats. Accordingly, a voltage of the string selection line SSL is raised by coupling according to voltage rise of the surface layer 114. For example, a voltage of the string selection line SSL rises up to a second string selection line voltage Vssl2.

At a third timing t3, a second word line erase voltage Vwe2 is applied to the word lines WL1 to WL3 of a selected sub block. For example, the second word line erase voltage Vwe2 is a low voltage. For example, a second word line erase voltage Vwe2 is a ground voltage Vss. At this point, a voltage of the surface layer 114 is a high voltage. Accordingly, Fowler-Nordheim (F-N) coupling is induced in memory cells of a selected sub block. Due to F-N tunneling, the memory cells MC1 to MC3 of a selected sub block are erased.

At a third timing t3, voltages of the word lines WL4 to WL6 of an unselected sub block have a level of a word line voltage Vwl. Exemplarily, the word line voltage Vwl is a voltage generated by coupling according to voltage rise of the surface layer 114. For example, the word line voltage Vwl is a high voltage. Exemplarily, the word line voltage Vwl prevents F-N tunneling from being induced in the word lines WL4 to WL6 of an unselected sub block. Accordingly, the word lines WL4 to WL6 of an unselected sub block are erase-inhibited.

At a third timing t3, a voltage of the ground selection line GSL has a level of a second ground selection line voltage Vgsl2. Exemplarily, the second ground selection line voltage Vgsl2 is a voltage is a voltage generated by coupling according to voltage rise of the surface layer 114. For example, the second ground selection line voltage Vgsl2 may be a high voltage. Exemplarily, a level of the second ground selection line voltage Vgsl2 is set in order not to prevent F-N from being induced tunneling in the ground selection transistor GST. For example, by adjusting a timing that the ground selection line GSL floats, a level of the second ground selection line voltage Vgsl2 may be adjusted. Accordingly, the ground selection transistor GST is erase-inhibited.

At a third timing t3, a voltage of the string selection line SSL has a level of the second ground selection line voltage

Vgsl2. Exemplarily, the second ground selection line voltage Vgsl2 is a voltage generated by coupling according to voltage rise of the surface layer **114**. For example, the second ground selection line voltage Vgsl2 may be a high voltage. Exemplarily, the second ground selection line voltage Vgsl2 prevents F-N tunneling from being induced in the string selection transistor SST. Accordingly, the ground selection transistor GST is erase-inhibited.

At the second and third timings t**2** and t**3**, a voltage of the dummy word line DWL maintains as the third dummy word line voltage Vdwl**3**. Exemplarily, a level of the third dummy word line voltage Vdwl**3** is set in order not to prevent F-N tunneling from being induced in the dummy memory cell DMC. Accordingly, the dummy memory cell DMC is erase-inhibited.

Exemplarily, a level of the third dummy word line voltage Vdwl**3** is set in order to prevent or reduce influence of coupling between the word lines WL**1** to WL**3** of a selected sub block and the word line WL**4** to WL**6** of an unselected sub block

For example, a voltage of the word lines WL**1** to WL**3** of a sub block selected at the third timing t**3** is lowered from the word line voltage Vwl to the second word line erase voltage Vwe. At this point, the third dummy word line voltage Vdwl**3** may be set, in order to prevent or reduce influence of coupling according to voltage drop of the word lines WL**1** to WL**3** of a selected sub block from being delivered to the word lines WL**4** to WL**6** of an unselected sub block. Moreover, the third dummy word line voltage Vdwl**3** may be set, in order to prevent or reduce influence of coupling of when a voltage of the word lines WL**4** to WL**6** of an unselected sub block is maintained from being delivered to the word lines WL**1** to WL**3** of a selected sub block.

Exemplarily, the third dummy word line voltage Vdwl**3** may have a level between the second erase voltage Vers**2** and the second word line erase voltage Vwe**2**. For example, the third dummy word line voltage Vdwl**3** may have a level between the word line voltage Vwl and the second word line erase voltage Vwe**2**.

In the above-mentioned example embodiments, it is described that the word lines WL**4** to WL**6** of an unselected sub block float. However, the second word line erase-inhibit voltage Vwei**2** may be applied to the word lines WL**4** to WL**6** of an unselected sub block. For example, at a first timing t**1**, a predetermined or desired voltage is applied to word lines of an unselected sub block. The predetermined or desired voltage may have a lower level than the second word line erase voltage Vwei**2**. Then, at a second timing t**2**, the second word line erase voltage Vwei**2** is applied to the word lines WL**4** to WL**6** of an unselected sub block.

Exemplarily, a level of the second word line erase voltage Vwei**2** may be set in order to prevent F-N tunneling from being induced through a voltage difference between the second word line erase voltage Vwei**2** and the second erase voltage Vers**2**.

Exemplarily, an equivalent circuit of the memory block BLKp may be illustrated as the equivalent circuit BLKi_**1** shown in FIG. **8**. Exemplarily, an equivalent circuit of the memory block BLKp may be illustrated as the equivalent circuits BLKi_**2** to BLKi_**8** shown in FIGS. **50** through **56**. That is, each NAND string of the memory block BLKp may include a lateral transistor LTR. At least one dummy memory cell DMC may be provided between sub blocks of the memory block BLKp. The number of memory cells DMC, which may be further provided between sub blocks of the memory block BLKp, may vary.

In each NAND string, at least two string selection transistors SST may be provided. In each NAND sting, at least two ground selection transistors GST may be provided. In each NAND string, at least one dummy memory cell DMC may be provided between the memory cells MC and the string selection transistor SST. In each NAND string, at least one dummy memory cell DMC may be provided between the memory cells MC and the ground selection transistor GST.

Exemplarily, as described with reference to FIGS. **48** and **49**, along the direction intersecting (for example, perpendicular to) the substrate **111** in each sub block, each of the first to last memory cells MC**1**, MC**3**, MC**4**, and MC**6** has a first size and each of the remaining memory cells MC**2** and MC**5** has a smaller second size than the first size.

For example, as described with reference to FIGS. **39** through **44**, instead of providing dummy memory cells DMC between sub blocks, a thickness of the insulation material **112'** between sub blocks may be formed greater than those of other insulation materials **112**.

For example, as described with reference to FIGS. **45** through **47**, dummy memory cells DMC are not provided, and along a direction intersecting (for example, perpendicular to) the substrate **111** in each sub block, each of the first to last memory cells MC**1**, MC**3**, MC**4**, and MC**6** has a first size and each of the remaining memory cells MC**2** and MC**5** has a smaller second size than the first size.

If the dummy memory cells DMC are not provided between sub blocks, voltage conditions and voltage changes during an erase operation of the memory block BLKo are the same as those shown in FIGS. **65** and **66**.

FIG. **65** is a table illustrating voltage conditions when dummy memory cells DMC are not provided between sub blocks of the memory block BLKp of FIGS. **43** and **44**. Except that a voltage condition of the dummy word line DWL is removed, the voltage conditions of FIG. **64** are the same as those of FIG. **63**.

FIG. **66** is a timing diagram illustrating a voltage change according to the voltage conditions of FIG. **65**. Except that a voltage change of the dummy word line DWL is removed, voltage changes of the FIG. **66** are the same as those of FIG. **64**.

Exemplarily, influence of coupling between sub blocks is prevented or reduced by the dummy word line DWL during a voltage change shown in FIG. **64** and also influence of coupling between sub blocks is prevented or reduced by an insulation material **112'** provided between sub blocks during a voltage change shown in FIG. **64**.

For example, as described with reference to FIGS. **18** through **20**, while a read operation is performed on a selected sub block among sub blocks of the memory block BLKp, each sub block of the memory block BLKp is selectively refreshed. For example, after data are written on a specific sub block of the memory block BLKp, when the number of reading operations on sub blocks of the memory block BLKp reaches a reference value, a specific sub block is refreshed.

As described in relation to FIGS. **21** to **38**, a refresh operation or a reclaim operation may be carried out by the memory block or the sub block.

FIG. **67** is a perspective view of one of the memory blocks BLK**1**-BLKz according to example embodiments of inventive concepts. FIG. **68** is a sectional view taken along the line LXVIII-LXVIII' of the memory block BLKq of FIG. **61**. Except that one pillar of the memory block BLKq includes a first sub pillar **113***a* and a second sub pillar **113***b*, the memory block BLKq has the same configuration as the memory block BLKp described with reference to FIGS. **61** through **62**.

As described with reference to FIGS. **57** and **58**, one pillar in the memory block BLKq includes a first sub-pillar **113***a* and a second sub-pillar **113***b*. The first sub pillars **113***a* and the second sub pillars **113***b* are the same as those described with reference to FIGS. **57** and **58**.

As described with reference to FIGS. **61** and **62**, an n-type doping region **315** forming a common source line CSL has a plate form.

Exemplarily, an erase operation of the memory block BLKq is performed according to the method described with reference to FIGS. **45** through **48**.

Exemplarily, an equivalent circuit of the memory block BLKq may be illustrated as the equivalent circuit BLKi_**1** shown in FIG. **8**. Exemplarily, an equivalent circuit of the memory block BLKq may be illustrated as the equivalent circuits BLKi_**2** to BLKi_**8** shown in FIGS. **50** through **56**. That is, each NAND string of the memory block BLKq may include a lateral transistor LTR. At least one dummy memory cell DMC may be provided between sub blocks of the memory block BLKq. The number of memory cells DMC, which may be further provided between sub blocks of the memory block BLKo, may vary.

In each NAND string, at least two string selection transistors SST may be provided. In each NAND sting, at least two ground selection transistors GST may be provided. In each NAND string, at least one dummy memory cell DMC may be provided between the memory cells MC and the string selection transistor SST. In each NAND string, at least one dummy memory cell DMC may be provided between the memory cells MC and the ground selection transistor GST.

Exemplarily, as described with reference to FIGS. **48** and **31**, along the direction intersecting (for example, perpendicular to) the substrate **111** in each sub block, each of the first to last memory cells MC**1**, MC**3**, MC**4**, and MC**6** has a first size and each of the remaining memory cells MC**2** and MC**5** has a smaller second size than the first size.

As described with reference to FIGS. **57** and **58**, first conductive materials **251**, **252**, and **253** having a height corresponding to the silicon pad SIP (i.e., a fifth height) form a dummy word line DWL and a dummy memory cell DMC. That is, the memory block BLKq may be divided into sub blocks based on a height corresponding to the silicon pad SIP.

For example, as described with reference to FIGS. **18** through **20**, while a read operation is performed on a selected sub block among sub blocks of the memory block BLKq, each sub block of the memory block BLKq is selectively refreshed. For example, after data are written on a specific sub block of the memory block BLKq, when the number of reading operations on sub blocks of the memory block BLKq reaches a reference value, a specific sub block is refreshed.

As described in relation to FIGS. **21** to **38**, a refresh operation or a reclaim operation may be carried out by the memory block or the sub block.

Exemplarily, it is described that a pillar includes a first sub pillar **113***a* and a second sub pillar **113***b*. However, a pillar may include at least two sub pillars.

FIG. **69** is a perspective view of one of the memory blocks BLK**1**-BLKz according to example embodiments of inventive concepts. FIG. **70** is a sectional view taken along the line LXX-LXX' of the memory block BLKr of FIG. **69**. Referring to FIGS. **69** and **70**, as described with reference to FIGS. **61** and **62**, an n-type doping region **315** forming a common source line CSL has a plate form.

Compared to the memory block BLKi described with reference to FIGS. **4** through **8**, a first conductive material **211***p* having a first height used for forming a ground selection line GSL has a plate form. First conductive materials **221***p* to **281***p* having second to eighth heights used for forming first to seventh word lines WL**1** to WL**7** have a plate form. First conductive materials **291***p*, **292***p*, and **293***p* having a ninth height used for forming a string selection line SSL extend along the first direction and are spaced apart from each other by a specific distance along the second direction.

A surface layer **116'** of each pillar **113'** includes an insulation layer. The surface layer **116'** of the pillar **113'** is configured to store data like the insulation layer **116** described with reference to FIG. **6**. For example, the surface layer **116'** may include a tunneling insulation layer, a charge storage layer, and a blocking insulation layer. A middle layer **114'** of the pillar **113'** includes a p-type silicon. The middle layer **114'** of the pillar **113'** operates as a body of the second direction. An inner layer **115'** of the pillar **113'** includes an insulation material.

Exemplarily, an erase operation of the memory block BLKr is performed according to the method described with reference to FIGS. **45** through **48**.

Exemplarily, an equivalent circuit of the memory block BLKr may be illustrated as the equivalent circuit BLKi_**1** shown in FIG. **8**. Exemplarily, an equivalent circuit of the memory block BLKr may be illustrated as the equivalent circuits BLKi_**2** to BLKi_**8** shown in FIGS. **50** through **56**. That is, each NAND string of the memory block BLKr may include a lateral transistor LTR. At least one dummy memory cell DMC may be provided between sub blocks of the memory block BLKr. The number of memory cells DMC, which may be further provided between sub blocks of the memory block BLKr, may vary.

In each NAND string, at least two string selection transistors SST may be provided. In each NAND sting, at least two ground selection transistors GST may be provided. In each NAND string, at least one dummy memory cell DMC may be provided between the memory cells MC and the string selection transistor SST. In each NAND string, at least one dummy memory cell DMC may be provided between the memory cells MC and the ground selection transistor GST.

For example, as described with reference to FIGS. **39** through **44**, instead of providing dummy memory cells DMC between sub blocks, a thickness of the insulation material **112'** between sub blocks may be formed greater than those of other insulation materials **112**.

For example, as described with reference to FIGS. **45** through **47**, dummy memory cells DMC are not provided, and along a direction intersecting (for example, perpendicular to) the substrate **111** in each sub block, each of the first to last memory cells MC**1**, MC**3**, MC**4**, and MC**6** has a first size and each of the remaining memory cells MC**2** and MC**5** has a smaller second size than the first size.

Exemplarily, as described with reference to FIGS. **48** and **49**, dummy memory cells DMC are provided between sub blocks and along the direction intersecting (for example, perpendicular to) the substrate **111** in each sub block, each of the first to last memory cells MC**1**, MC**3**, MC**4**, and MC**6** has a first size and each of the remaining memory cells MC**2** and MC**5** has a smaller second size than the first size.

For example, as described with reference to FIGS. **18** through **20**, while a read operation is performed on a selected sub block among sub blocks of the memory block BLKr, each sub block of the memory block BLKr is selectively refreshed. For example, after data are written on a specific sub block of the memory block BLKr, when the number of reading operations on sub blocks of the memory block BLKr reaches a reference value, a specific sub block is refreshed.

As described in relation to FIGS. **21** to **38**, a refresh operation or a reclaim operation may be carried out by the memory block or the sub block.

FIG. **71** is a perspective view of one of the memory blocks BLK**1**-BLKz according to example embodiments of inventive concepts. FIG. **72** is a sectional view taken along the line LXXII-LXXII' of the memory block BLKs of FIG. **71**. Except that one pillar of the memory block BLKs includes a first sub pillars **113***a* and a second sub pillars **113***b*, the memory block BLKs is the same as that described with reference to FIGS. **51** and **52**.

As described with reference to FIGS. **57** and **58**, one pillar in the memory block BLKs includes a first sub-pillar **113***a* and a second sub-pillar **113***b*. The first sub pillars **113***a* and the second sub pillars **113***b* are the same as those described with reference to FIGS. **57** and **58**.

Exemplarily, an equivalent circuit of the memory block BLKs may be illustrated as the equivalent circuit BLKi_**1** shown in FIG. **8**. Exemplarily, an equivalent circuit of the memory block BLKs may be illustrated as the equivalent circuits BLKi_**2** to BLKi_**8** shown in FIGS. **50** through **56**. That is, each NAND string of the memory block BLKs may include a lateral transistor LTR. At least one dummy memory cell DMC may be provided between sub blocks of the memory block BLKs. The number of memory cells DMC, which may be further provided between sub blocks of the memory block BLKs, may vary.

In each NAND string, at least two string selection transistors SST may be provided. In each NAND sting, at least two ground selection transistors GST may be provided. In each NAND string, at least one dummy memory cell DMC may be provided between the memory cells MC and the string selection transistor SST. In each NAND string, at least one dummy memory cell DMC may be provided between the memory cells MC and the ground selection transistor GST.

Exemplarily, as described with reference to FIGS. **48** and **49**, along the direction intersecting (for example, perpendicular to) the substrate **111** in each sub block, each of the first to last memory cells MC**1**, MC**3**, MC**4**, and MC**6** has a first size and each of the remaining memory cells MC**2** and MC**5** has a smaller second size than the first size.

As described with reference to FIGS. **57** and **58**, first conductive materials **251***p*, **252***p*, and **253***p* having a height corresponding to the silicon pad SIP (i.e., a fifth height) form a dummy word line DWL and a dummy memory cell DMC. That is, the memory block BLKs may be divided into sub blocks based on a height corresponding to the silicon pad SIP.

For example, as described with reference to FIGS. **18** through **20**, while a read operation is performed on a selected sub block among sub blocks of the memory block BLKs, each sub block of the memory block BLKs is selectively refreshed. For example, after data are written on a specific sub block of the memory block BLKs, when the number of reading operations on sub blocks of the memory block BLKs reaches a reference value, a specific sub block is refreshed.

As described in relation to FIGS. **21** to **38**, a refresh operation or a reclaim operation may be carried out by the memory block or the sub block.

Exemplarily, it is described that a pillar includes a first sub pillar **113***a* and a second sub pillar **113***b*. However, a pillar may include at least two sub pillars.

FIG. **73** is a perspective view of one of the memory blocks BLK**1**-BLKz according to example embodiments of inventive concepts. FIG. **74** is a sectional view taken along the line LXXIV-LXXIV' of the memory block BLKt of FIG. **73**. Referring to FIGS. **73** and **74**, first to fourth upper word lines UW**1** to UW**4** extending in the first direction are provided on a substrate **111**. The first to fourth upper word lines UW**1** to UW**4** are spaced a specific distance from each other along the second direction and first upper pillars UP**1** penetrating the first to fourth upper word lines UW**1** to UW**4** along the second direction are provided.

First to fourth lower word lines DW**1** to DW**4** extending along the first direction are provided on the substrate. The first to fourth lower word lines DW**1** to DW**4** are spaced apart from each other along the second direction. The first to fourth lower word lines DW**1** to DW**4** are spaced a specific distance from the first to fourth upper word lines UW**1** to UW**4** along a third direction.

First upper pillars DP**1** spaced a specific distance from each other along the first direction and penetrating the first to fourth lower word lines DW**1** to DW**4** along the second direction are provided. Moreover, second upper pillars DP**2** spaced a specific distance from each other along the first direction and penetrating the first to fourth lower word lines DW**1** to DW**4** along the second direction are provided. For example, the first lower pillars DP**1** and the second lower pillars DP**2** may be disposed parallel along the second direction. The first lower pillars DP**1** and the second lower pillars DP**2** are spaced a specific distance apart from each other along the third direction.

Fifth to eighth upper word lines UW**5** to UW**8** extending along the first direction are provided on the substrate **111**. The fifth to eighth upper word lines UW**5** to UW**8** are spaced a specific distance from each other along the second direction. The fifth to eighth upper word lines UW**5** to UW**8** are spaced a specific distance apart from the first to fourth lower word lines DW**1** to DW**4** along the third direction. Second upper pillars UP**2** spaced a specific distance apart from each other along the first direction and penetrating the fifth to eighth upper word lines UW**5** to UW**8** along the second direction are provided.

A common source line CSL extending in the first direction is provided on the top of the first and second lower pillars DP**1** and DP**2**. Exemplarily, the common source line CSL includes an n-type silicon material. Exemplarily, if the common source line CSL is formed of a conductive material without a conductive type such as an n-type or a p-type, n-type sources may be additionally provided between the common source line CSL and the first and second lower pillars DP**1** and DP**2**. For example, a region adjacent to the common source line CSL among regions of the first and second lower pillars DP**1** and DP**2** is doped with an n-type and thus may operate as a source. Exemplarily, each of the common source line CSL and the first and second lower pillars DP**1** and DP**2** may be connected through contact plugs. For example, the contact plugs are doped with an n-type and thus may operate as a source.

Drains **320** are provided on the tops of the first and second upper pillars UP**1** and UP**2**, respectively. Exemplarily, the drains **320** may include an n-type silicon material. A plurality of bit lines BL**1** to BL**3** extending along the third direction are provided o the tops of the drains **320**. For example, the bit lines BL**1** to BL**3** are spaced a specific distance apart from each other along the first direction. Exemplarily, the bit lines BL**1** to BL**3** are formed of metal. Exemplarily, the bit lines BL**1** to BL**3** and the drains **320** are connected through contact plugs (not shown).

Each of the first and second upper pillars UP**1** and UP**2** includes a surface layer **116"** and an inner layer **114"**. As illustrated with reference to FIGS. **51** and **52**, the surface layers **116"** of the first and second upper pillars UP**1** and UP**2** and the first and second lower pillars DP**1** and DP**2** may include a blocking insulation layer, a charge storage layer, and a tunneling insulation layer.

Exemplarily, the tunnel insulation layer includes a thermal oxide layer. The charge storage layer includes a nitride layer or a metal oxide layer (e.g., aluminum oxide layer, a hafnium oxide layer and so on). The blocking insulation layer is formed of a single layer or a multi layer. The blocking insulation layer may be a high dielectric layer (e.g., aluminum oxide layer, a hafnium oxide layer and so on) having a higher dielectric constant than the tunnel insulation layer and the charge storage layer. Exemplarily, the tunnel insulation layer, the charge storage layer, and the blocking insulation layer may constitute oxide-nitride-oxide (ONO).

Inner layers **114"** of the first and second upper pillars UP**1** and UP**2** and the first and second lower pillars DP**1** and DP**2** may include a p-type silicon material. The inner layers **114"** of the first and second upper pillars UP**1** and UP**2** and the first and second lower pillars DP**1** and DP**2** operate as a body of the second direction.

The first upper pillars UP**1** and the first lower pillars DP**1** are connected through first pipeline contacts PC**1**. Exemplarily, each of the surface layers **116"** of the first upper pillars UP**1** and the first lower pillars DP**1** are connected through the surface layers of the first pipeline contacts PC**1**. The surface layers of the first pipeline contacts PC**1** are formed of the same materials as the surface layers **116"** of the first upper pillars UP**1** and the first lower pillars DP**1**.

Exemplarily, each of the inner layers **114"** of the first upper pillars UP**1** and the first lower pillars DP**1** are connected through the inner layers of the first pipeline contacts PC**1**. The inner layers of the first pipeline contacts PC**1** are formed of the same materials as the inner layers **114"** of the first upper pillars UP**1** and the first lower pillars DP**1**.

That is, the first upper pillars UP**1** and the first to fourth upper word lines UW**1** to UW**4** form first upper strings, and the first lower pillars DP**1** and the first to fourth lower word lines DW**1** to DW**4** form first lower strings. Each of the first upper strings and the first lower strings is connected through the first pipeline contacts PC**1**. The drains **320** and the bit lines BL**1** to BL**3** are connected to one ends of the first upper strings. The common source line CSL is connected to one ends of the first lower strings. That is, the first upper strings and the first lower strings form a plurality of strings connected between the bit lines BL**1** to BL**3** and the common source line CSL.

Likewise, the second upper pillars UP**2** and the fifth to eighth upper word lines UW**5** to UW**8** form second upper strings, and the second lower pillars DP**2** and the first to fourth lower word lines DW**1** to DW**4** form second lower strings. Each of the second upper strings and the second lower strings is connected through the second pipeline contacts PC**2**. The drains **320** and the bit lines BL**1** to BL**3** are connected to one ends of the second upper strings. The common source line CSL is connected to one ends of the second lower strings. That is, the second upper strings and the second lower strings form a plurality of strings connected between the bit lines BL**1** to BL**3** and the common source line CSL.

Exemplarily, except that eight transistors are provided in one string and two strings are connected to each of the first to third bit lines BL**1** to BL**3**, an equivalent circuit of the memory block BLKt is the same as the BLKi_**1** of FIG. **8**. Additionally, except that eight transistors are provided in one string and two strings are connected to each of the first to third bit lines BL**1** to BL**3**, an equivalent circuit of the memory block BLKt is the same as the BLKi_**2** to BLKi_**8** of FIGS. **50** through **56**.

That is, each NAND string of the memory block BLKo may include a lateral transistor LTR. At least one dummy memory cell DMC may be provided between sub blocks of the memory block BLKo. The number of memory cells DMC, which may be further provided between sub blocks of the memory block BLKo, may vary. In each NAND string, at least two string selection transistors SST may be provided. In each NAND sting, at least two ground selection transistors GST may be provided. In each NAND string, at least one dummy memory cell DMC may be provided between the memory cells MC and the string selection transistor SST. In each NAND string, at least one dummy memory cell DMC may be provided between the memory cells MC and the ground selection transistor GST.

Exemplarily, in order to form channels in the inner layers **114"** in the first and second pipeline contacts PC**1** and PC**2**, first and second pipeline contact gates (not shown) may be provided respectively. Exemplarily, the first and second pipeline contact gates (not shown) may be provided on the surfaces of the first and second pipeline contacts PC**1** and PC**2**.

For example, the first and second pipeline contact gates (not shown) may correspond to the dummy memory cells DMC shown in FIG. **8**. That is, the memory block BLKt may be divided into sub blocks based on the first and second pipeline contact gates (not shown). Exemplarily, each of the first and second pipeline contact gates (not shown) may correspond to the two dummy memory cells DMC.

Exemplarily, it is described that the lower word lines DW**1** to DW**4** are shared in the adjacent lower pillars DP**1** and DP**2**. However, when the upper pillars adjacent to the upper pillars UP**1** and UP**2** are added along the third direction, the upper pillars adjacent along the third direction may be configured to share the upper word lines UW**1** to UW**4** or the upper word lines UW**5** to UW**8**. Exemplarily, the upper word lines UW**4** and UW**8** having the highest height among the upper word lines UW**1** to UW**4** or the upper word lines UW**5** to UW**8** adjacent along the third direction may be spaced a specific distance apart from each other.

Exemplarily, as described with reference to FIGS. **48** and **49**, along the direction intersecting (for example, perpendicular to) the substrate **111** in each sub block, each of the first to last memory cells MC**1**, MC**3**, MC**4**, and MC**6** has a first size and each of the remaining memory cells MC**2** and MC**5** has a smaller second size than the first size.

For example, as described with reference to FIGS. **18** through **20**, while a read operation is performed on a selected sub block among sub blocks of the memory block BLKo, each sub block of the memory block BLKo is selectively refreshed. For example, after data are written on a specific sub block of the memory block BLKo, when the number of reading operations on sub blocks of the memory block BLKo reaches a reference value, a specific sub block is refreshed.

As described in relation to FIGS. **21** to **38**, a refresh operation or a reclaim operation may be carried out by the memory block or the sub block.

In the above mentioned example embodiments, it is described that thicknesses of the first conductive materials forming the string selection transistor SST and the ground selection transistor GST are the same as those of the first conductive materials forming the memory cells MC in a sub block. However, thicknesses of the first conductive materials forming the string selection transistor SST and the ground selection transistor GST may be greater than those of the first conductive materials forming the memory cells MC in a sub block.

In the above mentioned example embodiments, it is described that a thickness of the insulation material **112** between the first conductive materials forming the string selection transistor SST and the first conductive materials forming the memory cells MC is the same as that of the insulation material **112** in a sub block. However, a thickness of the insulation material **112** between the first conductive materials forming the string selection transistor SST and the first conductive materials forming the memory cells MC may be greater than that of the insulation material **112** in a sub block.

In the above mentioned example embodiments, it is described that a thickness of the insulation material **112** between the first conductive materials forming the ground selection transistor GST and the first conductive materials forming the memory cells MC is the same as that of the insulation material **112** in a sub block. However, a thickness of the insulation material **112** between the first conductive materials forming the ground selection transistor GST and the first conductive materials forming the memory cells MC may be greater than that of the insulation material **112** in a sub block.

In the above mentioned example embodiments, it is described that selection transistors may have the same structure as memory cells that may include a first insulating layer, a charge trap layer, blocking layer and a gate electrode. Depending on the magnitude of a voltage applied to a gate electrode, selection transistors may perform the same function as memory cells. However, selection transistors need not have the same structure as memory cells. For example, selection transistors need not have charge trap layers or an active pillar.

FIG. **75** is a block diagram illustrating an application example of the memory system **1000** of FIG. **1**. Referring to FIG. **75**, a memory system **2000** includes a nonvolatile memory device **2100** and/or a controller **2200**. The nonvolatile memory device **2100** includes a plurality of nonvolatile memory chips. The plurality of nonvolatile memory chips are divided by groups. Each group of the nonvolatile memory chips is configured to communicate with the controller **2200** through one common channel. In FIG. **75**, it is illustrated that the plurality of nonvolatile memory chips communicate with the controller **2200** through first to kth channels CH**1** to CHk. Each nonvolatile memory chip has same configuration as the nonvolatile memory device **100** described with reference to FIGS. **1** through **74**.

Exemplarily, the controller **2200** is configured to control the nonvolatile memory device **2100**. For example, the controller **2200** is configured to control a refresh operation of the nonvolatile memory device **2100**. As described with reference to FIGS. **18** through **20**, the controller **2200** controls a refresh operation of the nonvolatile memory device **2100**.

The controller **2200** communicates with a plurality of nonvolatile memory chips through a plurality of channels. Accordingly, when a refresh operation is performed in one nonvolatile memory chip connected to a specific channel, nonvolatile memory chips connected to another channel continue in a standby state. That is, while a refresh operation is performed in one nonvolatile memory chip connected to one channel, operations such as writing, reading, and erasing may be performed in the nonvolatile memory chip connected to another channel.

FIG. **76** is a block diagram illustrating a computing system **3000** with the memory system **2000** described with reference to FIG. **75**. Referring to FIG. **76**, the computing system **3000** includes a central processing unit (CPU) **3100**, a random access memory (RAM) **3200**, a user interface **3300**, a power supply **3400**, a system bus **3500** and/or the memory system **2000**.

The memory system **2000** is electrically connected to the CPU **3100**, the RAM **3200**, and the power supply **3400** through the system bus **3500**. Data provided through a user interface **3300** or processed by the CPU **3100** are stored in the memory system **2000**. The memory system **2000** includes a controller **2200** and a nonvolatile memory device **2100**.

In FIG. **76**, it is illustrated that the nonvolatile memory device **2100** is connected to the system bus **3500** through the controller **2200**. However, the nonvolatile memory device **2100** may be directly connected to the system bus **3500**. At this point, the CPU **3100** controls a refresh operation of the nonvolatile memory device **2100**.

In FIG. **76**, it is described that the memory system **200** described with FIG. **75** is provided. However, the memory system **2000** may be replaced with the memory system **1000** described with FIG. **1**.

Exemplarily, the computing system **3000** may be configured to include all the memory systems **1000** and **2000** described with reference to FIGS. **1** and **75**.

According to example embodiments of inventive concepts, a memory block includes a plurality of sub blocks and performs an erase operation by a sub block unit. Since a merge unit is reduced, a nonvolatile memory device having an improved operating speed, an operating method of the same, and a memory system including the same may be provided.

According to example embodiments of inventive concepts, a sub block is refreshed according to the number of reading operations on a memory block after data are written into sub blocks. Since the number of reading operations on another sub block in the same memory block is considered, a nonvolatile memory device having an improved operating speed, an operating method of the same, and a memory system including the same may be provided.

According to example embodiments of inventive concepts, a dummy memory cell is provided at an interface of adjacent sub blocks. Since a medium voltage is applied to a dummy word line connected to a dummy memory cell, coupling between sub blocks is reduced. Accordingly, a nonvolatile memory device having an improved operating speed, an operating method of the same, and a memory system including the same may be provided.

According to example embodiments of inventive concepts, a distance between memory cells provided at an interface of adjacent sub blocks is longer than that between memory cells in each sub block. Since coupling between sub blocks is reduced, a nonvolatile memory device having an improved operating speed, an operating method of the same, and a memory system including the same may be provided.

According to example embodiments of inventive concepts, a size of a memory cell provided at the outline of a sub block is greater than that of a memory cell provided in the sub block. Since coupling between a memory cell at the outline of the sub block and a channel is enhanced, a nonvolatile memory device having an improved operating speed, an operating method of the same, and a memory system including the same may be provided.

The above-disclosed subject matter is to be considered illustrative, and not restrictive, and the appended claims are intended to cover all such modifications, enhancements, and other embodiments, which fall within the true spirit and scope of the present invention. Thus, to the maximum extent allowed by law, the scope of the present invention is to be determined by the broadest permissible interpretation of the following claims and their equivalents, and shall not be restricted or limited by the foregoing detailed description.

What is claimed is:

1. A method of operating a nonvolatile memory device that includes a substrate and memory blocks having a plurality of memory cells stacked along a direction perpendicular to the substrate, the method comprising:

reading data from a selected sub block among sub blocks of a selected memory block; and

selectively refreshing each sub block of the selected memory block in response to the reading of the selected sub block,

wherein each sub block of the selected memory block is separately erased.

2. The method of claim **1**, wherein the selectively refreshing of each sub block of the selected memory block in response to the reading of the selected sub block comprises, when the number of reading operations performed in the selected memory block reaches a reference value after data are written into a specific sub block among sub blocks of the selected memory block, refreshing the specific sub block.

3. The method of claim **1**, wherein the selectively refreshing of each sub block of the selected memory block in response to the reading of the selected sub block comprises:

backing up data of a specific sub block among sub blocks of the selected memory block; and

erasing the specific sub block.

4. The method of claim **3**, wherein the backing up of the data of a specific sub block among sub blocks of the selected memory block comprises:

reading data of the specific sub block; and

writing the read data into a sub block among sub blocks of the memory blocks.

5. The method of claim **3**, wherein the erasing of the specific sub block comprises:

applying a word line erase voltage to word lines corresponding to the specific sub block among word lines of the selected memory block;

floating the remaining word lines of the selected memory block; and

applying an erase voltage to the substrate.

6. The method of claim **5**, wherein the erasing of the specific sub block further comprises applying a medium voltage to at least one dummy word line between the specific sub block and at least one sub block adjacent to the specific sub block.

7. The method of claim **6**, wherein the medium voltage has a level between the word line erase voltage and the erase voltage.

8. The method of claim **3**, wherein the erasing of the specific sub block comprises:

applying a word line erase voltage to word lines corresponding to the specific sub block among word lines of the selected memory block;

applying a word line erase-inhibit voltage to the remaining word lines of the selected memory block; and

applying an erase voltage to the substrate.

9. A nonvolatile memory device comprising:

a memory cell array including a substrate and memory blocks, the memory blocks including a plurality of memory cells stacked along a direction perpendicular to the substrate;

a decoder connected to the memory blocks through word lines; and

a read and write circuit connected to the memory blocks through bit lines, wherein each memory block is divided into a plurality of sub blocks along a direction perpendicular to the substrate,

each sub block is separately erased,

memory cells in each sub block are spaced from each other by a first distance, along the direction perpendicular to the substrate, and

memory cells at an interface of sub blocks adjacent along the direction perpendicular to the substrate are spaced from each other by a longer second distance than the first distance.

10. The nonvolatile memory device of claim **9**, wherein in each sub block, each of the first and last memory cells has a first size along the direction perpendicular to the substrate and each of the remaining memory cells has a second size smaller than the first size.

11. The memory system of claim **9**, wherein

the plurality of memory cells in each memory block are organized into a plurality of NAND strings,

each one of the plurality of NAND strings includes a plurality of first memory cells stacked on top of each other and a plurality of second memory cells stacked on top of each other between a ground selection transistor and a string selection transistor,

the second memory cells is on top of the first memory cells, and

the string selection transistor is on top of the ground selection transistor,

the plurality of sub-blocks in each memory block include a first sub-block including the plurality of first memory cells and a second-sub block including the plurality of second memory cells.

12. The memory system of claim **11**, wherein each one of the plurality of NAND strings includes a dummy memory cell between the plurality of first memory cells and the plurality of second memory cells.

13. The memory system of claim **11**, wherein

each one of the plurality of NAND strings includes an insulating layer between the plurality of first memory cells and the plurality of second memory cells, and

a thickness of the insulating layer is greater than a vertical distance between the first memory cells.

14. The memory system of claim **11**, further comprising:

a plurality of bit lines

a common source line, wherein

the plurality of NAND strings are each electrically connected to the common source line and a corresponding one of the plurality of bit lines.

15. A memory system comprising:

a nonvolatile memory device including a substrate and memory blocks, the memory blocks having a plurality of memory cells stacked along a direction perpendicular to perpendicular to the substrate; and

a controller controlling the nonvolatile memory device,

wherein each memory block is divided into a plurality of sub blocks along the direction perpendicular to the substrate;

each sub block is separately erased; and

based on the number of reading operations performed on a selected memory block among the memory blocks, the controller selectively refreshes each sub block of the selected memory block.

16. The memory system of claim **15**, wherein when the number of reading operations performed on the selected memory block reaches a reference value after data are written into a selected sub block of the selected memory block, the controller selectively refreshes each sub block of the selected memory block.

17. The memory system of claim **15**, wherein when a specific sub block among sub blocks of the selected memory block is refreshed, the controller reads data of the specific sub block and writes the read data into one of sub blocks of the memory blocks.

18. The memory system of claim **15**, wherein in each memory block, at least one dummy memory cell is provided between sub blocks adjacent along the direction perpendicular to the substrate.

19. The memory system of claim **15**, wherein the nonvolatile memory device and the controller constitute a solid state drive (SSD).

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